DEVELOPMENT OF A READOUT SYSTEM FOR A HIGH RATE MICRON RESOLUTION SINGLE PHOTON UV IMAGING DETECTOR

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ABSTRACT

Ultraviolet (UV) photon detection in astronomical applications requires detectors capable of single photon counting at Megahertz event rates with high spatial resolution and very low noise. NASA, through their Strategic Astrophysics Technology (SAT) program, has funded the development of a cross strip (XS) microchannel plate (MCP) detector along with the corresponding read-out electronics with the intention to increase its technology readiness level (TRL), thus enabling prototyping of such systems/detectors for future NASA missions.

The detectors designed for measuring low intensity light (single photons) must be robust against fluctuating count rates, have very good spatial resolution (µm range), and contribute very low background noise to the image. These requirements lead toward the development of custom Application Specific Integrated Circuits (ASICs), which are able to read the signals from the detector, while contributing a minimal amount of noise to the system. The readout system described in this work has been designed with the intent to replace the original 19-inch rack-mounted, high-powered electronics with ASICs in order to lower the power, mass, and volume requirements of the detector electronics, which are all very limited resources in space applications. Thus a collaboration between the Space Science Laboratory at University of Berkeley and the Instrumentation Development Laboratory (IDLab) at the University of Hawaii at Manoa has been established, in which IDLab is responsible for the development of the read-out electronics.

This thesis presents the design, fabrication, and testing of the ASICs required for the readout system. In the first phase, a 16-channel trans-impedance amplifier ASIC (CSAv3) was designed and developed; this component converts the collected charge from the detector into a measurable voltage pulse. These pulses are subsequently transferred upon and digitized by a waveform sampling ASIC (HalfGraph2). The post processing of the acquired information is done on field programmable gate arrays (FPGAs) and the results are transferred to a computer for analysis. After successfully completing the first phase, the second phase is to further integrate the readout system by combining the CSAv3 and HG2 chips into one high-density, low power, front-end mixed-signal amplifier/digitizing ASIC, denoted as GRAPH, with further improvements to the design of the individual parts to decrease the material budget, lower the power consumption, improve the performance, and ultimately reduce the physical footprint of the electronics.

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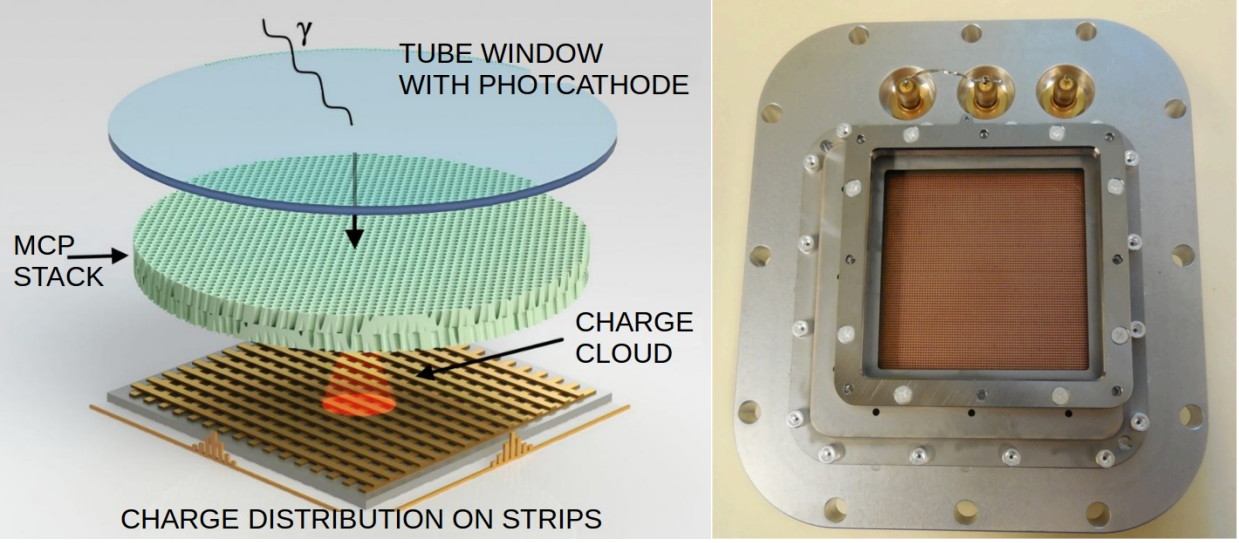
CHAPTER 1
INTRODUCTION

Over the last three decades, many astronomical research experiments studying the formation of stars and stellar systems in the UV wavelength band of electromagnetic spectrum (10-400 nm) have been based on photon counting micro channel plate (MCP) imaging detectors. Approximately 65% of the volume of the interstellar medium (ISM) is filled with diffuse gas at very high temperatures (between 3000 K and 300 000 K). This gas is best observed in the UV spectrum. Some of the experiments studying this are the Extreme Ultraviolet Explorer (EUVE), the Far Ultraviolet Spectroscopic Explorer (FUSE), and the Cosmic Origins Spectrograph on the Hubble telescope (COS on HUBBLE) [5] [6] [2]. In addition, such UV detection systems have been mentioned to be the choice of instruments on future large telescopes in space missions such as Large UV/Optical/Infrared Surveyor (LUVOIR) [7]. The readout electronics described in this work are developed for very similar detector applications using cross strip (XS) MCP technology, with an intention to increase NASAs technology readiness level, thus enabling prototyping for future space missions.

1.1 Detector operation

The photon detection principle is based on the photoelectric effect, where an incident photon hits the photocathode and releases an electron. The electron is then accelerated under a strong electric field, due to the high voltage applied over the MCP stack, as shown in Figure 1.1a. The multiplication of electrons is achieved by colliding them with the porous MCP structure. The resulting amplification is in order of 10^6 and the resulting cloud of electrons is then deposited upon a patterned XS anode array, consisting of 80 x 80 strips with a pitch of 625 µm, yielding into an active detection area of 50 x 50 mm^2. Figures 1.1a and 1.1b present a schematic of the MCP detector with the principle of operation and the picture of the actual detector, respectively [1] [3].



(a) (b)

Figure 1.1: (a) Schematic of the single photon detector operation. As the photon hits the photocathode, an electro is released and accelerated under electric field. As the electron collides with the MCP stack, as the electron hits the MCP structure, more electrons are released. The resulting cloud of electrons is then deposited upon a patterned XS anode array [1] [2] [3]. (b) Picture of the detector [2].

1.2 Principle of measurement

Measuring the charge deposited on the anode strips for a single event allows the extrapolation of the centroid of the charge cloud, leading to the photon entrance position. To optimize this measurement, each anode strip needs to be read out separately. However, using discrete components for the implementation of a readout system for such a large number of channels is impractical and thus leads into the development of custom ASICs. Each measurement channel is composed of the circuits presented in Figure 1.2:

1. A charge sensitive amplifier (CSA), which converts the input charge into a voltage pulse of proportional amplitude.
2. A pole-zero cancellation (PZC) circuit, which introduces a zero at the time constant of the CSA integrator, thus reducing the tail of the RC signal, and thereby enabling higher count rates without pile up.
3. A shaper, which optimizes the output pulse between the rise time and the noise.
4. An analog-to-digital converter (ADC), which digitizes the voltage pulses.

5. A field programmable gate array (FPGA), which processes the digitized data and reconstructs the photon position.

6. A computer, which stores and displays the acquired information.

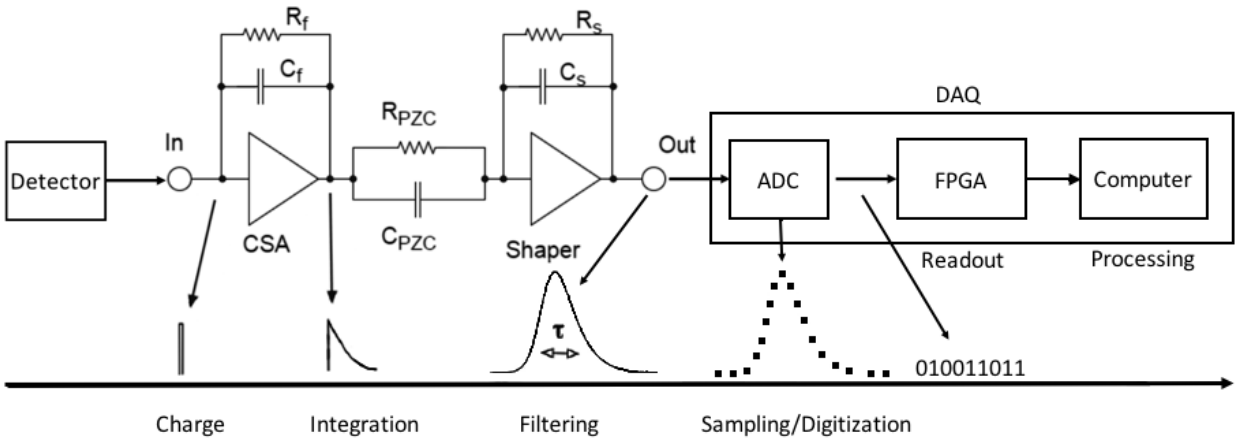


Figure 1.2: The schematic of a single channel of the signal processing chain. The charge cloud induced by the detector is integrated by the capacitor of the CSA feedback network, generating a potential across the capacitor. The output of the amplifier adjusts to maintain the anode at ground potential via feedback network, thus converting the input charge to an output voltage. The shaping amplifier, together with the PZC circuitry, optimizes the shape of the output pulse for readout. The digitizer samples the pulse and transmits it outside the chip for post-processing [1] [3].

CHAPTER 2
CHARGE SENSITIVE AMPLIFIER - CSAV3 ASIC

The first stage of the readout system for the XS MCP detector is a 16-channel charge sensitive amplifier (CSA) ASIC, denoted as CSAv3, designed and fabricated in 130 nm TSMC CMOS technology [1].

2.1 Amplifier principle of operation and construction

The CSA ASIC is composed of the following stages: a charge sensitive input amplifier, a pole zero cancellation circuit, a shaping amplifier, a programmable voltage amplifier, an analog multiplexer, and an output buffer. The first three stages are discussed in detail in the upcoming sections.

2.1.1 Charge Sensitive Amplifier

The CSA is a single ended, folded cascode connected amplifier with a feedback network composed of parallel resistor and capacitor connection (RC feedback); the schematic view of the classical implementation of the CSA is shown in Figure 2.1 [1] [3].

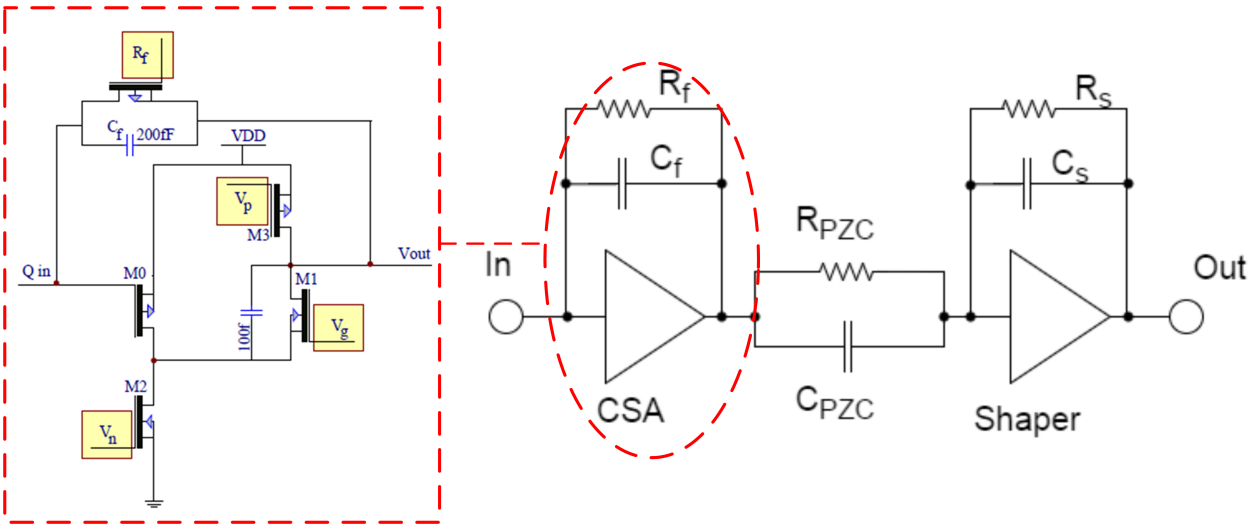


Figure 2.1: CSA chematic [1] [3].

The charge cloud induced by the MCP stack is collected by the XS anode array, where each strip is DC-coupled to a CSA channel input. The charge is then collected by the capacitor of the feedback network generating a potential across the capacitor. The output of the amplifier adjusts to maintain the anode at ground potential via feedback network, thus converting the input charge to an output voltage. The relation between the input charge and the voltage output of the CSA is

given in Equation 2.1, where the Q_i represents the input charge, C_f the feedback capacitance, and V_{out} the output voltage [1] [3].

$$Q_i = C_f \times V_{out} \equiv V_{out} = \frac{Q_i}{C_f} \tag{2.1}$$

The resistor of the feedback network discharges the feedback capacitor, thus controlling the return of the output signal to its baseline by following the time constant presented in Equation 2.2.

$$\tau = R_f \times C_f \tag{2.2}$$

The transfer function of the CSA in Laplace domain is presented in Equation 2.3; the convention used here follows the parameters indicated in the classical implementation of the CSA as presented in Figure 2.1.

$$H_{CSA}(s) = -\frac{R_f}{1 + sC_fR_f} \tag{2.3}$$

2.1.2 Pole Zero Cancellation Circuit

Due to the long time constant of the CSA feedback network, the return to the baseline time from the amplifier output pulse may cause the events to overlap, thus limiting the maximum event rate of the system. In order to mitigate this effect, called pile-up, a PZC circuit is implemented. This circuit consists of a parallel combination of resistor and capacitor, which can be expressed as an input impedance to the shaper, where the resistor is a PMOS transistor working in a linear region, hence allowing adjustability for the circuit. The PZC time constant is aimed to match the RC time constant of the CSA to obtain the best result. The PZC circuit is presented in the second stage from left in Figure 2.1 [1] [3].

2.1.3 Shaping Circuitry

The shaping amplifier, together with the PZC circuitry, is used to control the shape of the output pulse and the gain of the system. The amplifier is constructed from an operational transconductance amplifier (OTA) with programmable gain and shaping options. The gain and the shaping parameters are controlled with an analog multiplexer along with the controllable PZC resistance. The transfer function for the combined PZC circuitry and the shaper is given in the Equation 2.4; the transfer functions in this section are presented in the Laplace domain [1] [3].

$$H_{PZC+Shaper}(s) = -\frac{1 + sC_{PZC}R_{PCZ}}{R_{PZC}} \frac{R_S}{1 + sC_SR_S} \tag{2.4}$$

By combining the transfer functions presented in Equations 2.3 and 2.4, the transfer function for the whole amplifier/shaping signal chain is acquired as presented in Equation 2.5.

$$H(s) = -\frac{R_f}{1 + sC_f R_f} * \left(-\frac{1 + sC_{PZC} R_{PCZ}}{R_{PZC}} \frac{R_S}{1 + sC_S R_S} \right) \tag{2.5}$$

By setting the PZC circuit values to match the values in CSA feedback network as expressed in Equation 2.6, the long time constant of the CSA can be removed and replaced with a shorter time constant as shown in Equation 2.7 [1] [3].

$$C_{PZC} R_{PCZ} = C_f R_f \tag{2.6}$$

$$H(s) = \frac{R_f}{R_{PCZ}} \times \frac{R_S}{1 + sC_S R_S} \tag{2.7}$$

After the shaping circuitry, the signal is additionally amplified by using an OTA in inverting configuration, which allows the invertion of the originally negative pulse into positive.

2.2 CSAv3 ASIC design

2.2.1 Amplifier specifications

The electrical performance specifications for the CSAv3 ASIC are listed in Table 2.1 [1].

Table 2.1: Summary of the achieved CSAv3 ASIC specifications [1].

	Specification
Linear dynamic range	0-60 fC (AC or DC coupled)
Baseline device capacitance	5 pF
Amplifier gain	10 $\frac{mV}{fC}$
Noise at 5 pF detector capacitance	$< 1000\ e^-$
Shaping time	rise time 20 ns, pulse contained within 100 ns
Equivalent Noise Charge (ENC)	$\leq 1000\ e^-$ at 5 pF detector capacitance
Output load	5 nH, 5 pF, 100 $k\Omega$
Maximum event rate	1 MHz
Pulse width	$< 100\ n$s
Linear headroom without compression	600 mV
Power consumption	$\approx$ 5 mW/Ch

In addition to the specifications listed in Table 2.1, the ASIC has:

1. Programmable gain, shaping time, and the polarity of the signal.
2. Possibility for read-back of the programmable settings.

3. Verification option for the signals inside the amplifier chain.

4. Amplifier chain charge injection option for testing purposes.

2.2.2 Amplifier construction

The amplifier chain for a single ASIC channel is presented in Figure 2.2. In addition to the amplifier implementation presented in Figure 2.1, this topology adds two more stages: an analog multiplexer, responsible for selecting the amplification and polarity of the output signal and an output buffer, used for driving the signal outside the chip.

The yellow boxes in Figure 2.1 indicate the programmable parameters of the circuit. These parameters are used for selecting between different resistor and capacitor values and setting bias voltages by using programmable 12-bit digital-to-analog converters (DACs); the resistor and capacitor values are set via one 16-bit digital register and the bias voltages via ten separate DACs. The system is programmed by a 4-wire serial bus, reading and writing settings. In addition, the circuit allows for charge injection into the amplifier chain, which can be used for testing purposes [1] [3].

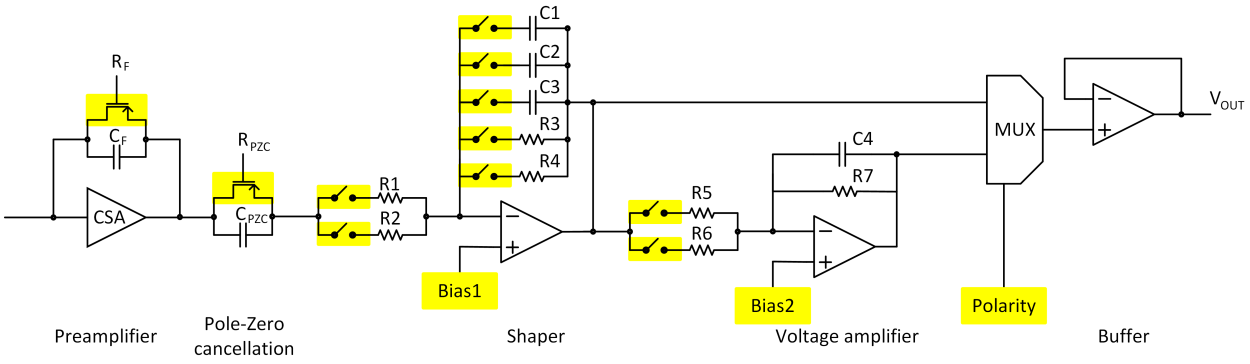


Figure 2.2: Schematic of the amplifier chain. The yellow boxes indicate the programmable resistor, capacitor, and bias options.

2.2.3 Amplifier and ASIC layout

The layout of the amplifier chain and the full ASIC are presented in Figures 2.3 and 2.4 respectively. The 16 channels are stacked vertically with digital controls at the bottom of the circuit. The loading mechanism is oriented perpendicularly (at the right) for optimal wiring. The final size of the ASIC die is approximately 3.4 $\times$ 3.4 mm^2 and it fits inside a 8.3 $\times$ 8.3 mm^2, 68 pin quad flat no-lead package (QFN68) [1] [3].

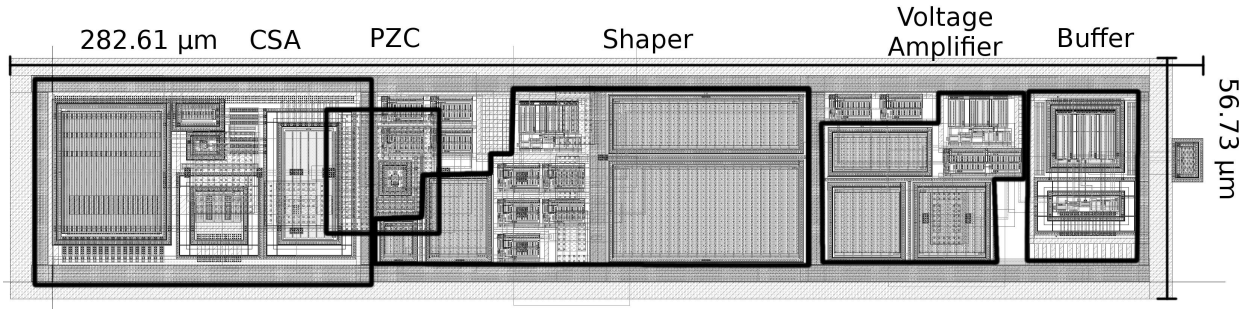


Figure 2.3: CSAv3 channel layout [1].

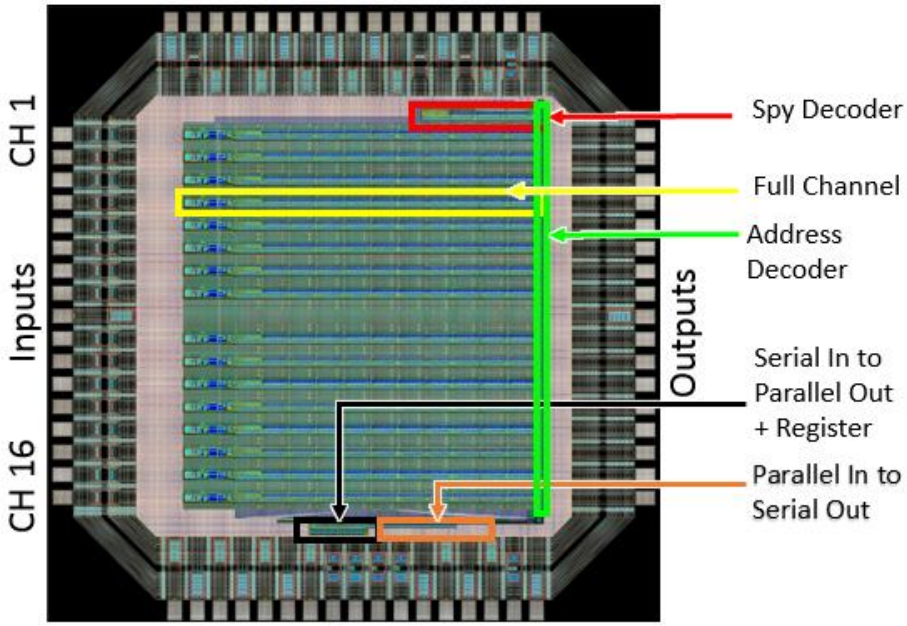


Figure 2.4: CSAv3 layout image [1].

2.3 Results

The chip was tested on an evaluation printed circuit board (PCB) with decoupled ground planes to reduce noise from the digital lines. An oscilloscope was used to measure the amplifier response using a probe with different impedance loading characteristics from the requirements. The testing was performed in the following stages:

1. The amplifier channel response as a function of time for a 50 fC charge, as presented in Figure 2.5a [1].

2. The gain linearity response as presented in Figure 2.5b. The average gain for the simulation is 10.396 mV/fC with mean squared linearity error of 0.13 mV/fC. The measured data shows an average gain of 9.4 mV/fC and mean square linearity error of 0.36 mV/fC [1].

3. The noise as a function of detector capacitance as presented in Figure 2.5c. This measurement was performed by changing capacitor values on the input and measuring the voltage RMS value on the output. The result indicates an equivalent noise charge (ENC) of approximately 600 e^- at 0 pF input capacitance; the ENC was calculated as shown in Equation 2.8.

$$ENC = -\frac{\frac{V_{RMS}}{Gain}}{1.6 \times 10^{-19} As} \tag{2.8}$$

   The discrepancies between the simulated and the measured results are attributed from the loading of the measuring probe, oscilloscope limitations, and bandwidth of the system; more specifically, both the parasitic capacitances from the test board and the loading from the probes limits the available bandwidth, thus contributing to the noise slope. However, it should be noted that the measured performance is better than the simulated [1].

4. The gain spread due to the process variations, evaluated by performing a Monte Carlo analysis, as presented in Figure 2.5d. The measured gain distribution over 32 channels shows the mean value of 9.4 mV/fC and sigma of 0.36 mV/fC [1].

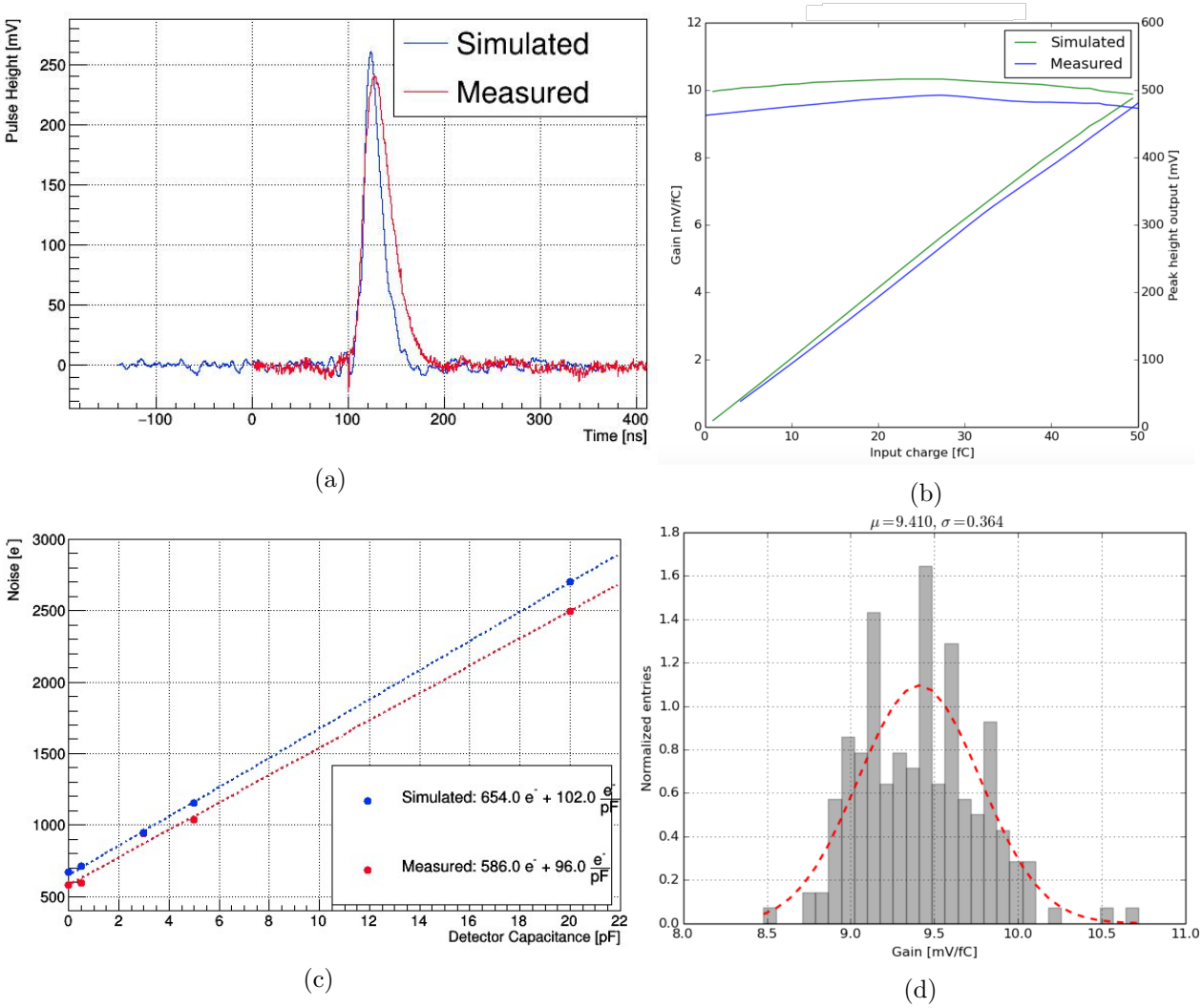


Figure 2.5: (a) Simulated and measured amplifier response for a 50 fC of charge as a function of time [1]. (b) Gain linearity of the CSA as a function of injected charge [1]. (c) Simulated and measured noise as a function of detector capacitance [1]. (d) Measured gain distribution of the CSA [1].

CHAPTER 3
WAVEFORM SAMPLER/DIGITIZER - HALFGRAPH2 ASIC

The second stage of the readout system is a 12- bit Giga Sample Per Second (GS/s) waveform sampling/digitizing ASIC called HalfGraph2 (HG2), developed in the TSMC 250 nm CMOS technology node. Its purpose is to sample and digitize the waveform output of the CSAv3. In addition, the channel count of the HG2 matches the channel count of the CSAv3, thus providing high scalability of the number of channels.

The HG2 consists of seven main blocks shown in Figure 3.1:

1. Triggering circuit: Transmits a pulse to the FPGA as a channel crosses an adjustable threshold to indicate that an event occurred.
2. Timing generator: Provides a common sampling time base for all channels.
3. Sampling array: Temporary memory, composed of switched capacitors.
4. Storage array: Provides analog buffering for the sampled analog values. Every channel has been8192 storage cells, arranged as 256 banks of 32 samples.
5. Wilkinson ADC: Digitizes the analog samples held in the storage array.
6. Output multiplexer: Selects the digitized channels.
7. Low voltage differential signaling (LVDS) transmitters: Transmits the digitized data off-chip in a high-speed, low-power differential manner.

The specifications for HG2 ASIC are listed in Table 3.1.

Table 3.1: Summary of the achieved HG2 ASIC specifications.

	Specification
Input channels	16
Sampling rate	1 GS/s
Dynamic range	1.8 V
Memory	8 µs
Wilkinson ADC clock	≈ 500 MHz
ADC resolution	Adjustable 8-12 bits
Event rate	1 MHz
Trigger outputs	4+1 (hit channel encoded)

3.1 Waveform digitizer/sampling ASIC

3.1.1 Principle of operation

HG2 continuously samples the input signal into a cyclically overwritten sampling array. As an event occurs, the trigger circuitry of the HG2 transmits a pulse to the FPGA. Upon a trigger event, the samples from the sampling window are transferred to the storage array continuously. The dead time from transferring the sampled data is mitigated by using an interleaved sampling scheme with two sampling windows, where one window is sampling, while the other is transferring data and vice-versa. The samples are digitized by the Wilkinson ADC. The digitized data is shifted out to the FPGA for readout and post processing. The block diagram of HG2 is presented in Figure 3.1.

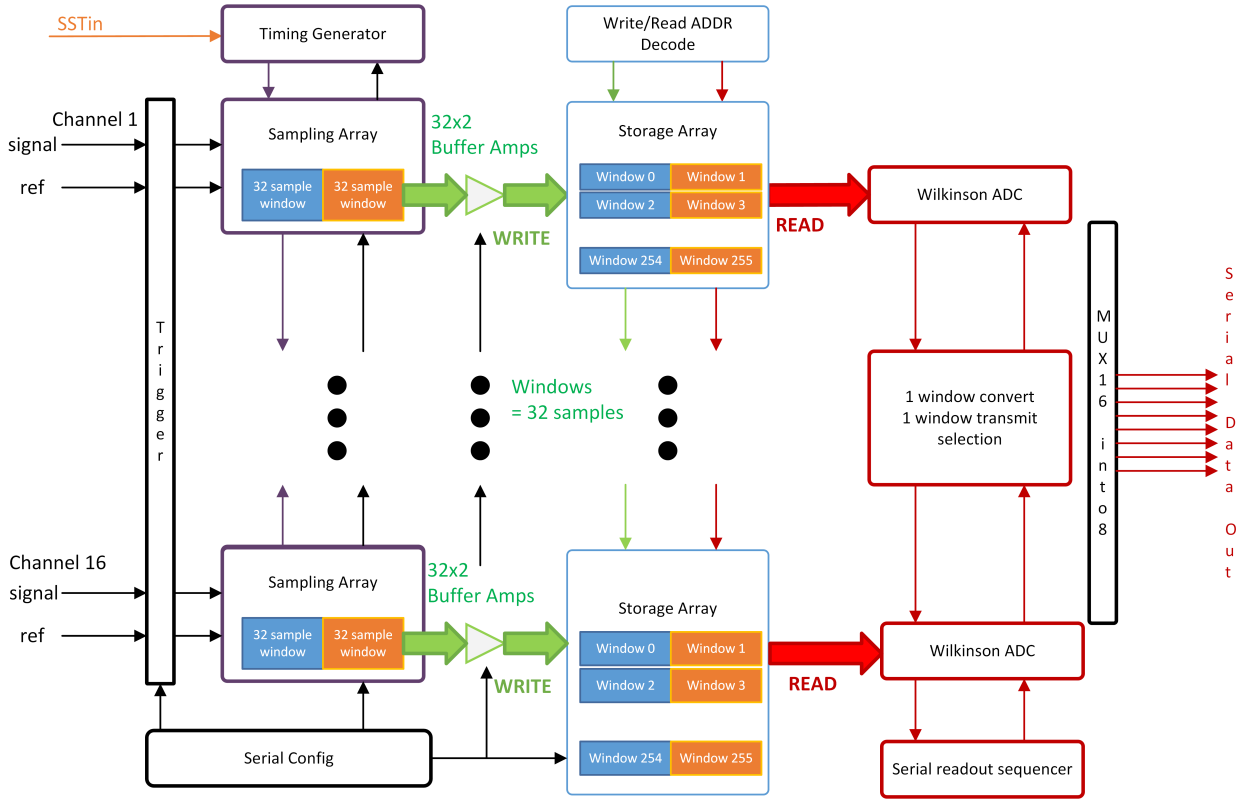


Figure 3.1: HG2 functional block diagram. When a signal of interest enters the digitizer input, the trigger circuitry transmits a pulse to the FPGA. At the same time sampling array samples the signal. The sampled signal is buffered into the storage array, where it is digitized by using the wilkinson ADC. The digitized signal is transferred outside the chip by LVDS drivers.

3.1.2 Trigger circuitry

The trigger circuit of the HG2 detects the edges of the input signal independently from the rest of the sampling circuitry. Its output is a fast indicator of a significant input pulse and is used by the FPGA to initiate the digitization and the readout of the corresponding relevant samples in the HG2 storage array. In order to be able to adjust the trigger circuit to various input signals, the trigger threshold, trigger polarity, and the output pulse width are adjustable. The top level block diagram of the HG2 trigger circuit is illustrated in Figure 3.2.

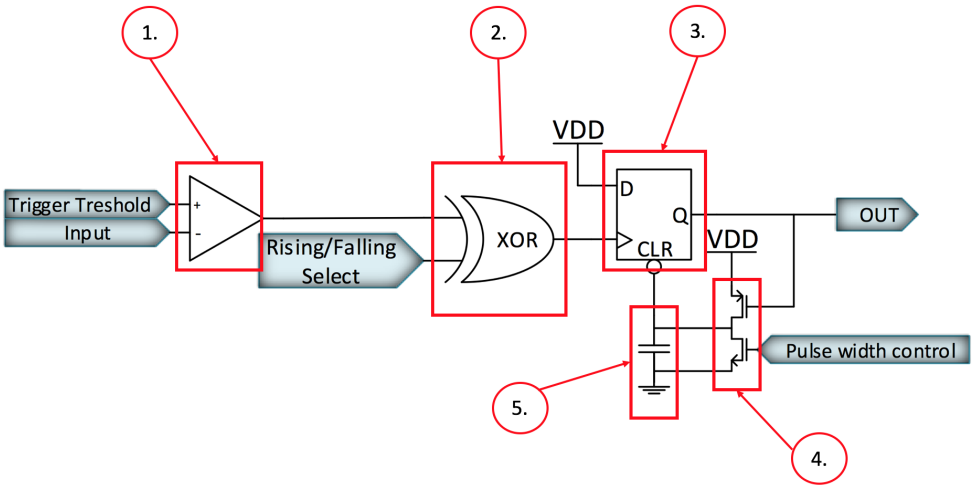


Figure 3.2: Trigger circuit functional block diagram.

The circuit is divided in five subsections:

1. The first stage is a comparator, made of an OTA operating in open loop, which directly compares a given channel input to a programmable threshold voltage.

2. The second stage is an XOR circuit, in which the comparator output is routed and is used for inverting the comparator edge depending on its select line input.

   (a) If select line = 0, the output reacts in rising edge.

   (b) If select line = 1, the output reacts in falling edge.

3. The third stage is a self-resetting D-Flip Flop (DFF), which is used along with stages 4 and 5 to form a feedback loop to generate a logical output pulse of configurable length between 10 µs to 150 µs, independent of the input pulse length.

3.1.3 Timing generator

The timing generator is used for generating a common time base for all sampling cells and is composed of an even number of delay cells, as presented in Figure 3.3. One delay cell is constructed

from two current starved inverters, that can be adjusted, and a capacitor, which acts as a load that generates a rise time and thus generates the delay. The adjustable inverters are used due to their ability for timing correction. The correction is done by a phase detector that controls a charge pump. The phase detector compares the input signal with the output signal from any chosen delay cell; this signal is denoted as SSToutFB and it is user selectable. The phase difference between these two signals are compared and the resulting signal drives the charge pump, which in turn provides with the control voltage for the delay elements; this topology is denoted as delay locked loop. The output of the charge pump adjusts the triggering level of the first inverter inside the delay cell and thus corrects the timing. Additional precision can be achieved by adjusting the second inverter with an external DAC.

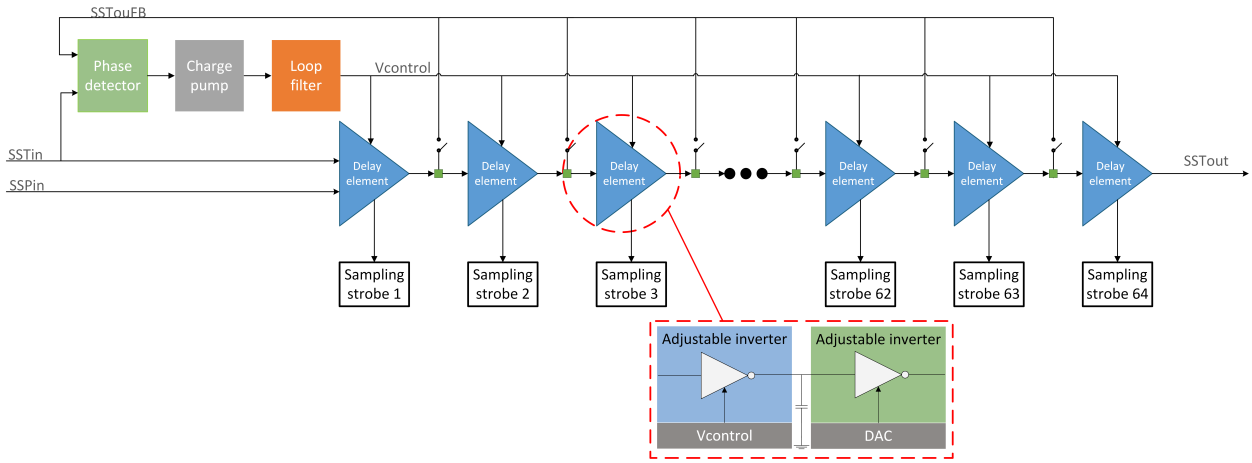


Figure 3.3: Timing generator functional block diagram. The SSTin and SSPin signals control the track and hold time of the sampling cells. SSToutFB signal, together with SSTin, controls the phase detector, which corrects the the timing errors. Each delay cell is provided with an adjustable inverter, which can be trimmed for extra accuracy if needed.

The operation of the timing generator in time domain is shown in Figure 3.4. In order to operate properly, two input signals are needed: SSTin and SSPin, where both signal need to be operated at the same clock frequency. The sampling operates as follows:

1. The sampling/tracking of the signal starts when the SSTin is set to low and SSPin to high, meaning that the sampling capacitor is charged into a current value of the input signal.

2. As the SSTin signal is set to high, the sampling switch is closed and the value is stored into the sampling capacitor.

3. The pulse width of the SSPin signal determines the tracking time of the sampling stage.

4. The sampling time is controlled by the phase detector. By choosing the SSToutFB properly, the delay cell triggers can be controlled to have correct pulse width. This can be trimmed even more accurately by internal DACs inside the delay cells.

5. Since the data in HG2 is acquired at 1 GSPS rate, the SSTin needs to be clocked with 15.625 MHz (1 GHz / 64 samples) speed and the difference between samples needs to be 1 ns. With this rate, all 64 samples are taken in one clock period and as new clock sequence starts, the sampling sequence is repeated.

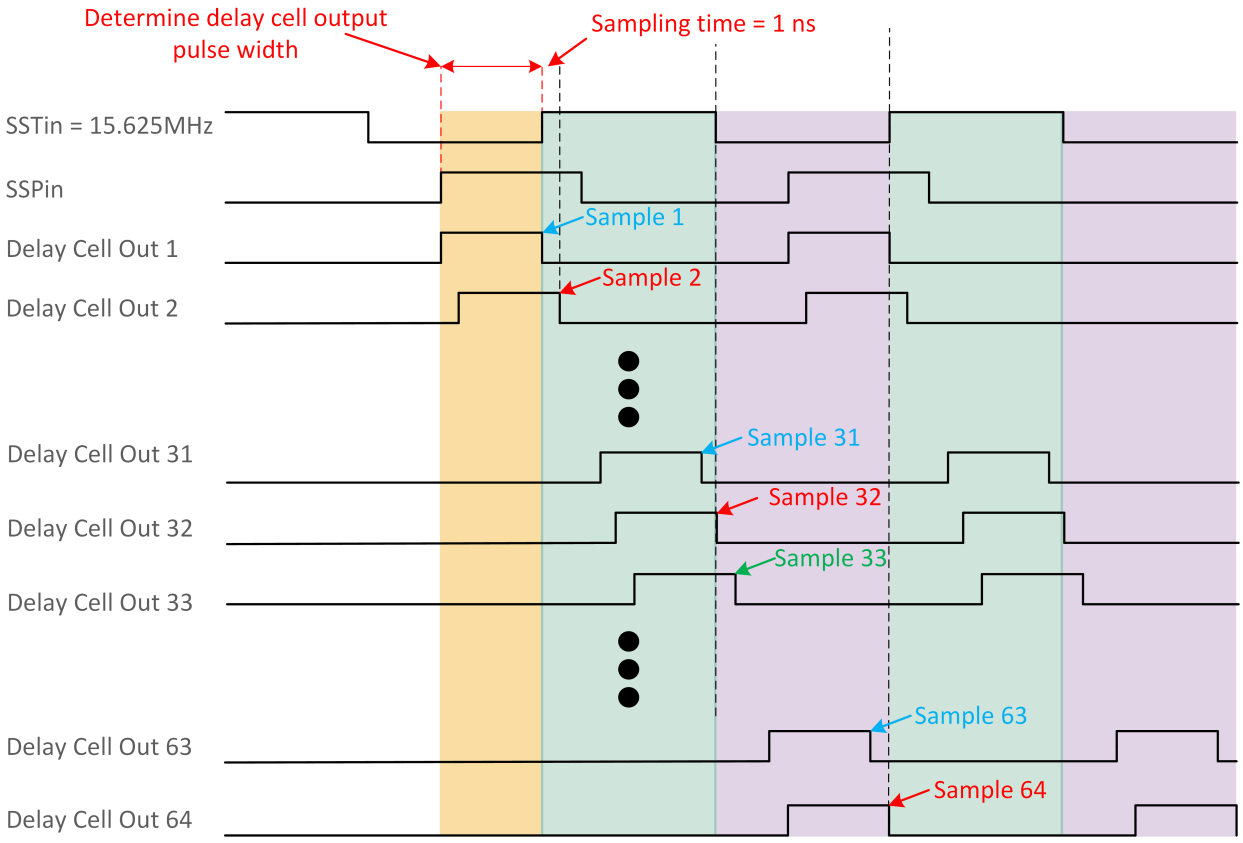


Figure 3.4: Timing generator functional block diagram. SSTin and SSPin signals control the track/hold time of the sampling. As the first sample is triggered, the signal triggers the next delay cell and so on, until all 64 samples are taken and sampling is restarted.

3.1.4 Sampling array

The sampling array is a temporary storage for the sampled signals. It consists of two windows with 32 sampling cells each for each individual channel; the sampling cell in HG2 consists of a switch, a capacitor, and a buffer amplifier. The samples are taken in an interleaved sampling scheme, where

one 32-sample window is sampling and at the same time another window is transferring the samples into the storage array, thus mitigating the dead time. Figure 3.5 presents a block diagram view of the sampling array.

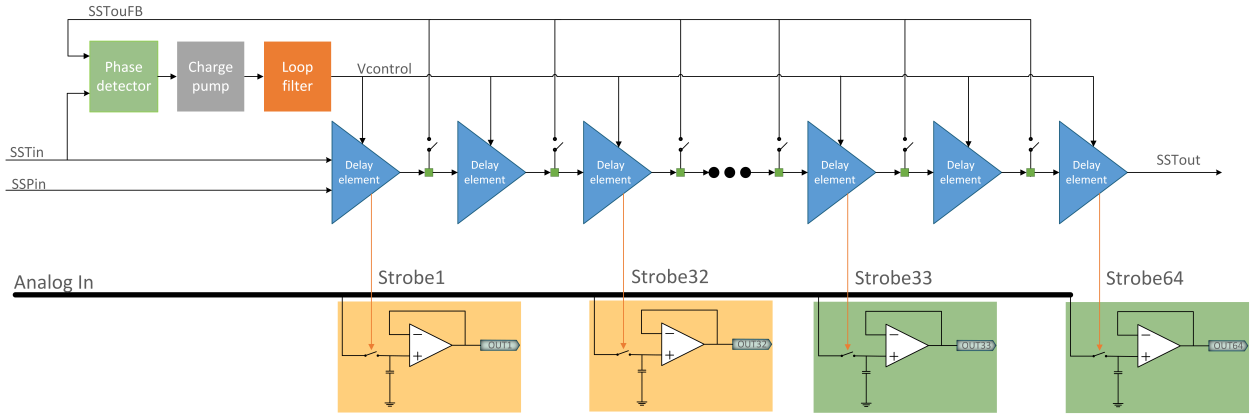


Figure 3.5: Functional block diagram of the sampling Array.

3.1.5 Storage array

The storage array is the long-term memory for the signals acquired from the sampling array. The construction of the storage cell is very similar to the sampling cell. A single storage cell consists of a switch, a storage capacitor, and a comparator, which will be used together with the Wilkinson ADC to digitize the sampled voltage stored in the capacitor. A schematic view of a single storage cell is presented in Figure 3.6.

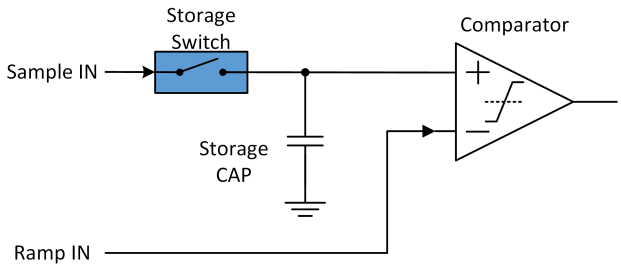


Figure 3.6: HG2 storage cell schematic view.

The full storage array consists of 256 storage windows, 32 samples each, leading into 8192 storage cells for each channel, which is equivalent to 8.192 µs of memory. The 256 windows are divided into two interleaved sections, where one half is used for collecting the sampled information from the sampling cells, while the other, together with Wilkinson ADC, is used for digitizing the stored information. The storage array needs to be large enough to prevent the sampled data overflow

during the digitization, which compared to the sampling speed, is a slow process. In HG2, the digitization time is data size dependent, however, the average digitization time is 7 µs, which allows some headroom for larger data sets.

3.1.6 Wilkinson ADC

The Wilkinson ADC is used for digitizing the stored analog samples into digital domain by using the time to digital conversion. The ADC consists of a ramp generator, a counter, and a register; the operational block diagram is presented in Figure 3.7. The HG2 has a single ramp generator and counter available for every storage cell in a chip, which run continuously to digitize the data from the storage cells. The output of each comparator is connected into a register, where the digitized data is stored.The Wilkinson ADCs operates as follows:

1. The stored sample is applied directly to the inverting input of its comparator.
2. A synchronous, linear analog ramp voltage is generated and connected into the non-inverting input of comparator and the clock counter is enabled.
3. When the sampled analog voltage equals the ramp voltage, the comparator changes state and the counter is frozen.
4. The counter value is stored into a local register at the comparator trigger event, which also marks the end of one conversion.
5. The data is shifted outside the chip serially.
6. The measurement of interest is obtained by multiplying the counter output word by the slope of the ramp (volt/clock-cycle).

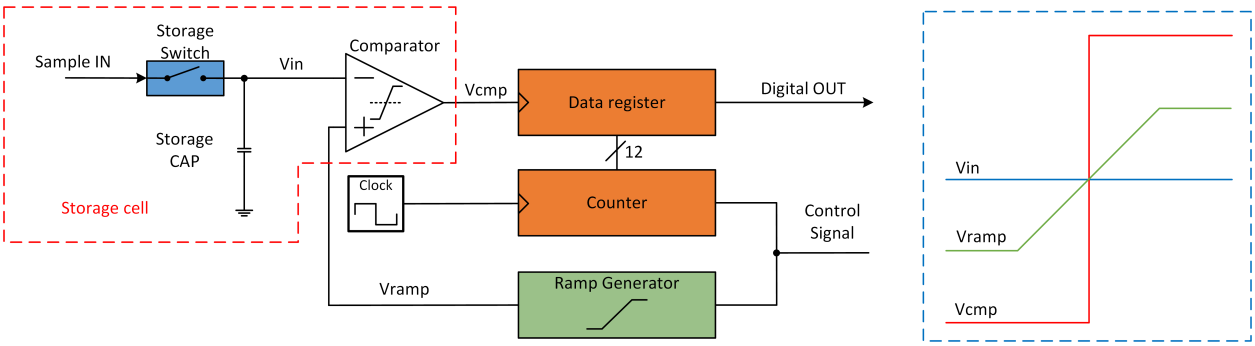
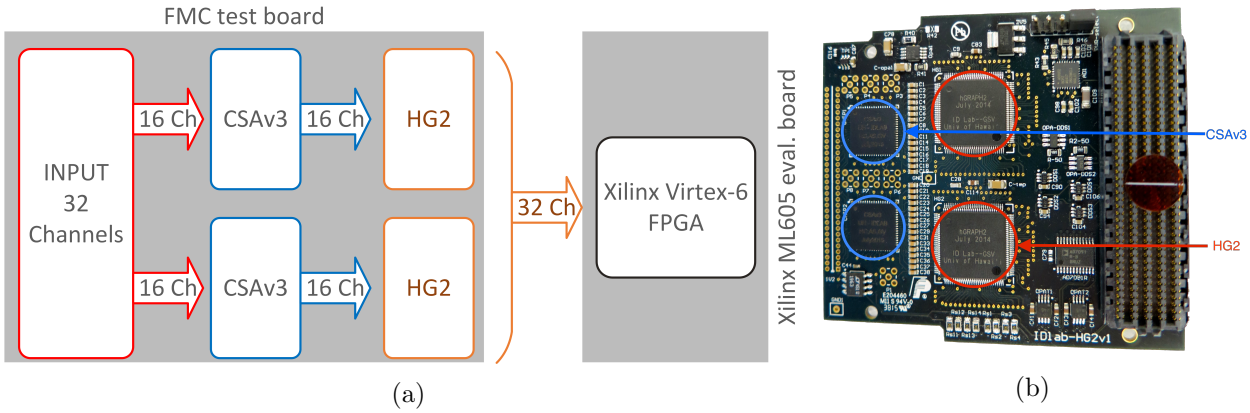


Figure 3.7: Wilkinson ADC operational block diagram. The storage capacitor is connected to the inverting input of the comparator and the ramp voltage is connected to the non-inverting input of the comparator. When the ramp voltage is larger than the stored voltage, the comparator output changes state. When the comparator trigger event happens, the counter value is saved in the data register, which is eventually shifted outside the chip.

3.2 Test board

In order to test the HG2 chips, a test board was designed by using the FPGA Mezzanine Standard (FMC). The FMC standard was chosen because they can be directly coupled with a variety of commercially available evaluation boards. In this case a Xilinx ML605 evaluation board was used for testing purposes due to its large Xilinx Virtex-6 XC6VLX240T-1FFG1156 FPGA [8]. The purpose of the FMC test board is to evaluate the performance of a small scale readout system by testing a small set of channels with an ability for setting the test charge injection values and calibration for the time base. The test setup provides two CSAv3 ASICs and two HalfGRAPH2 ASICs, which provides 32 readout channels in total. The 3.8b shows the picture of the actual test board and Figure 3.8a illustrate its block diagram.

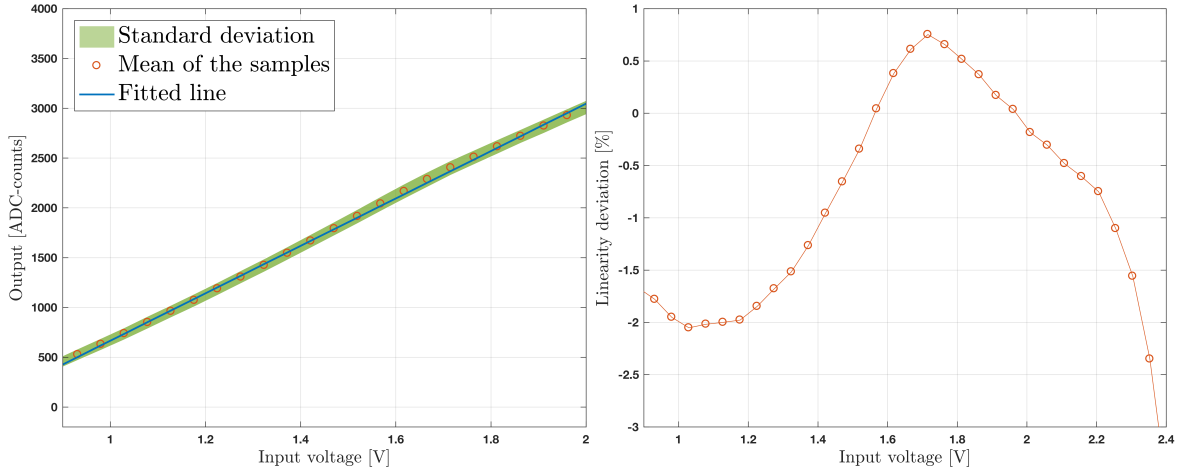


(a) (b)

Figure 3.8: (a) Test board setup block diagram. (b) FMC test board.

3.3 Results

An FMC evaluation board has been developed and used for a variety of performance tests. One such test is the evaluation of the HG2 input linearity. In this linearity test, DC input voltages in the range of 0 V to 2.5 V are applied to all channel inputs and sampled into each storage cell of the chip. This yields the response function in digitized ADC values as a function of input voltage for each individual memory cell of the ASIC. The result of the response linearity measurement is presented in Figures 3.9a and 3.9b. For each input voltage, the red circles in Figure 3.9a show the mean digitized value of all memory samples. The green area in Figure 3.9a represents the standard deviation of all memory samples for a given input voltage. The data points are fitted with a linear function in the range of 1 V to 2 V using a least square method. The fit line is presented as the blue line in Figure 3.9a. The extracted differences between the fit and the data points is presented in Figure 3.9b.



(a) (b)

Figure 3.9: (a) Mean response function for one HG2 channel with sample standard deviation and linear fit. (b) Deviation from linear fit line of the HG2.

The usable dynamic range of the HG2 is approximately from 1 V to 2 V. Below 1 V, the HG2 comparator input transistors operates in the linear region and thus the data below this level is non-linear. This can be improved by re-designing the comparator to have rail-to-rail input common mode operation; this is the first of the improvements of GRAPH ASIC and it is presented in Section 4.1.2. The samples above 2 V are non-linear because the ramp generator current source cannot hold itself in saturation anymore due to the channel length modulation. This can be improved by re-designing the current source with high output impedance, which mitigates the effect of channel length modulation, thus improving the upper end saturation level; this is the second improvement of the GRAPH ASIC, presented in Section 4.1.3. The deviation from the linear response is no more than 2 % in the fitted range from 1 V to 2 V.

CHAPTER 4
GRAPH - ASIC

The GRAPH ASIC integrates the CSAv3 and HG2 ASICs on a single die in order to further minimize the power consumption, material budget, and improve upon the overall performance of the readout system. Because the current HG2 is built in 250 nm technology, the whole digitization part has to be re-designed to be compliant with the 130 nm process. As CMOS devices are scaled to smaller sizes, the power supply rails, channel lengths, and gate oxide thicknesses decrease. This leads to new design challenges. Consequently, new design approaches must be considered in order to achieve the desired performance. The block diagram of the GRAPH ASIC is presented in Figure 4.1 [9].

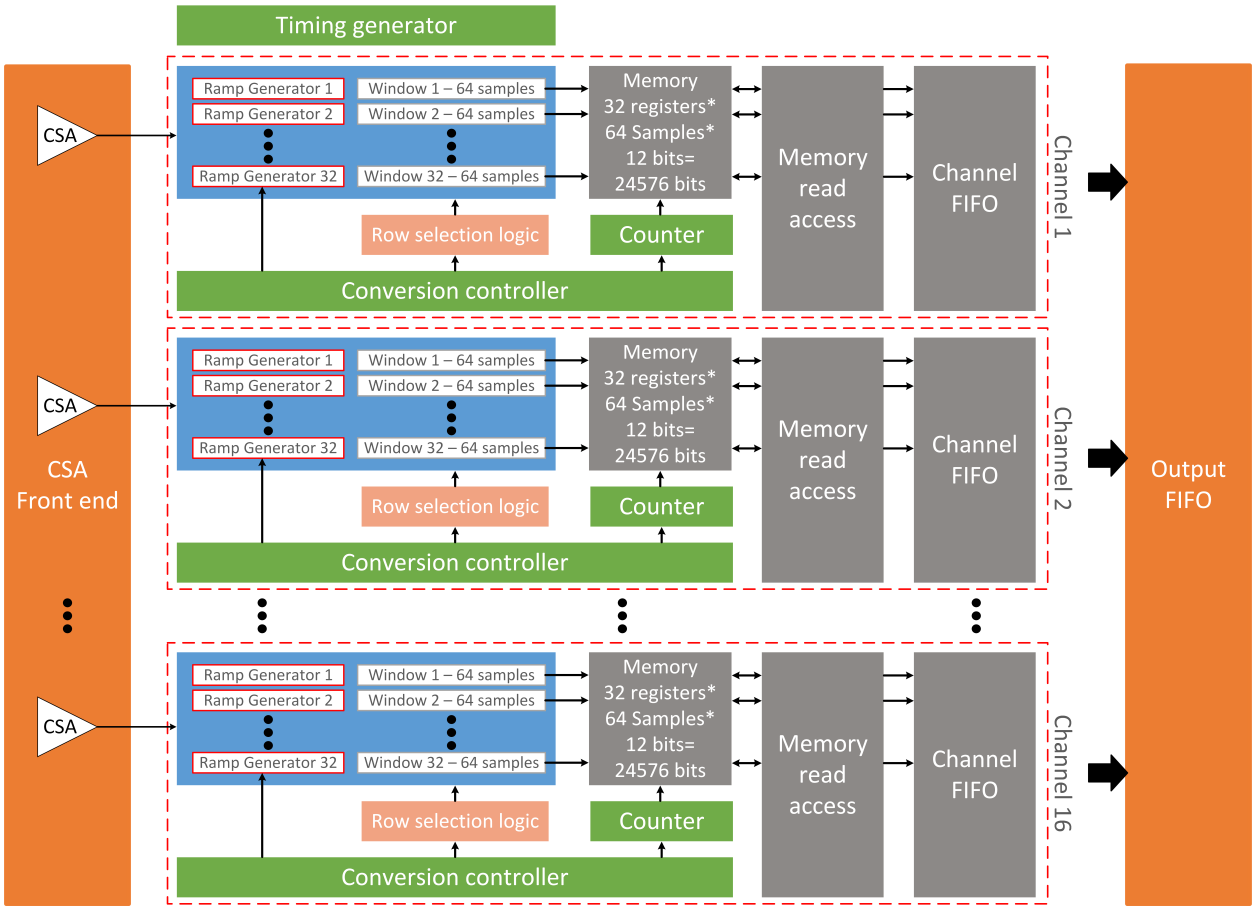


Figure 4.1: Block diagram of the GRAPH ASIC.

In the GRAPH ASIC, one of the major challenges is the larger leakage current resulting from

smaller transistor dimensions. A more detailed analysis of the leakage current is presented in Section 4.1.1. Consequently, employing a similar data storage principle as in the HG2 ASIC, where the information is stored as charge on capacitors, is no longer viable [9]. In this chapter, a completely new sampling structure, that is designed to satisfy the requirements and at the same overcome the leakage problem, is introduced and discussed. This new structure is still based on switched capacitor arrays (SCA), however, the transferring of sampled data to a storage array has been replaced with direct digitization of the samples. The digitized data is then stored in a digital memory buffer, which does not suffer from leakage issues.

The GRAPH ASIC features 16 channels with a sampling speed of 1 GS/s and a total power consumption of approximately 0.5 W. In order to provide some flexibility, CSA front-end and the digitized back-end will have the ability for decoupling one from another, thus operating independently. That is, the GRAPH will have the ability to function as standalone sampler and digitizer. The rest of the GRAPH target specifications are listed in Table 4.1.

Table 4.1: Summary of the GRAPH ASIC target specifications.

	Specification
Input channels	16
Sampling rate	1 GS/s
Digitizer dynamic range	800 mV
Sample conversion	64 samples in parallel
Wilkinson ADC clock	$\approx$ 500 MHz
ADC resolution	Adjustable 8-12 bits
Digitization time	$\approx 1\,\mu s$
Trigger outputs	4
Power consumption	$\approx$ 0.5 W/channel

4.1 Sampling Unit Design

Each of the 16 channels has a dedicated sampling unit composed of 32 sampling arrays with each sampling array composed of 64 sampling cells; all 32 arrays are driven by one delay-locked loop (DLL). Each sampling cell is made of an input switch (transmission gate), sampling capacitor, and a comparator, where the comparator is part of the Wilkinson ADC. Apart from the comparators, the Wilkinson ADC has one ramp generator and one 12-bit counter per sampling array. A simplified block diagram of the the GRAPH sampling unit is shown in Figure 4.2

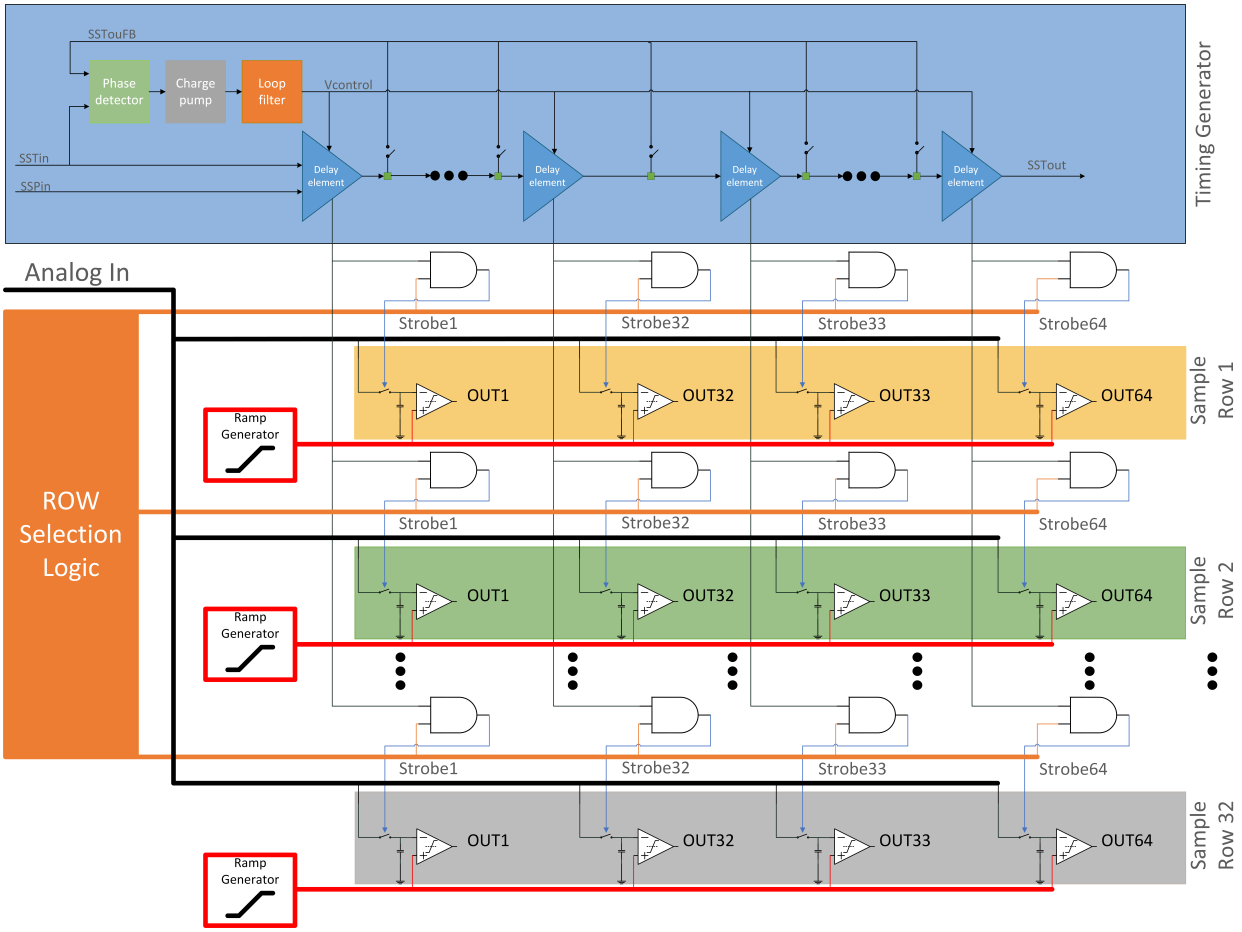


Figure 4.2: Block diagram of the GRAPH ASIC sampling unit.

Apart from solving the leakage issue, an important advantage of such a topology is the ability to prevent dead time between digitization cycles. That is, as one SCA is sampling, the others are all in hold mode and ready for digitization.

4.1.1 Sampling cell design

The sampling cell consists of a parallel combination parallel combination of NMOS and PMOS transistors, forming a voltage controlled complementary switch, denoted as transmission gate, and a sampling capacitor. Figure 4.3 shows a schematic view of the sampling cell [10].

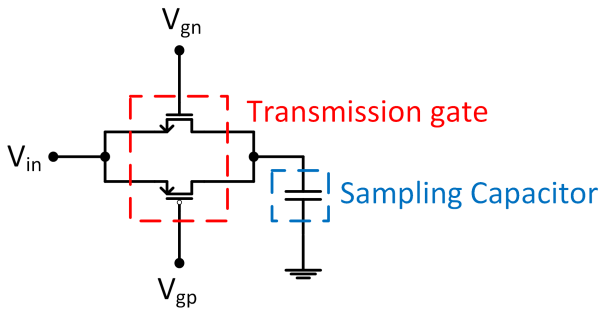


Figure 4.3: Schematic view of one sampling cell.

To determine the optimal value for the sampling capacitor, three key performance parameters needs to be evaluated. These parameters are the sampling capacitor value, switch on-state/off-state resistance and switch on-state bandwidth.

In hold mode, the noise on the sampling capacitor is dominated by the "kT/C-noise", which is caused by the thermal agitation of the charge carriers on the sampling capacitor. More specifically, the charge carriers on the capacitor plates travel between the voltage source and the capacitor due to their random thermal energies, causing the voltage across the capacitor to fluctuate over time. The RMS noise voltage is calculated using Equation 4.1, where k is the Boltzmann's constant (1.38×10^{-23} AVs/K), T is the absolute temperature in Kelvins, and C is the sampling capacitance. The noise as a function of capacitor value and temperature is shown in Figure 4.4 [10] [11].

$$V_{rms-noise} = \sqrt{\frac{kT}{C}} \tag{4.1}$$

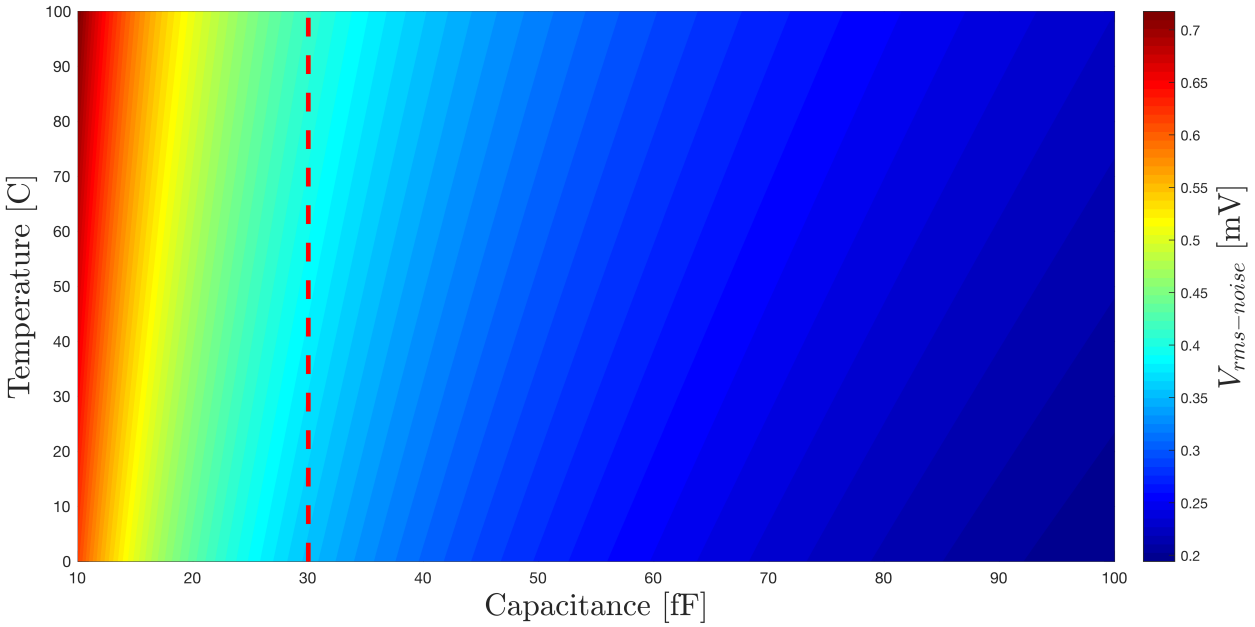


Figure 4.4: Noise as a function of temperature and sampling cell capacitance.

The noise voltage can only be reduced by either operating in very low temperatures or by implementing a larger sampling capacitor value. The operating temperature of the chip is hard to accurately characterize during the design phase, thus the capacitor needs to be sized such that the kT/C noise contribution remains within the required noise tolerances of the system.

Ultimately, the system bandwidth should not be limited by the RC time constant (τ) of the transmission gate on-state resistance and the sampling capacitor. The target specifications for the GRAPH ASIC require the sampling speed to be 1GS/s. Consequently, by following the Nyquist theorem, the system bandwidth should not exceed 500 MHz. The simulation result for the transmission gate on-state resistance (r_{on}) as a function of BW and capacitance is presented in Figure 4.5.

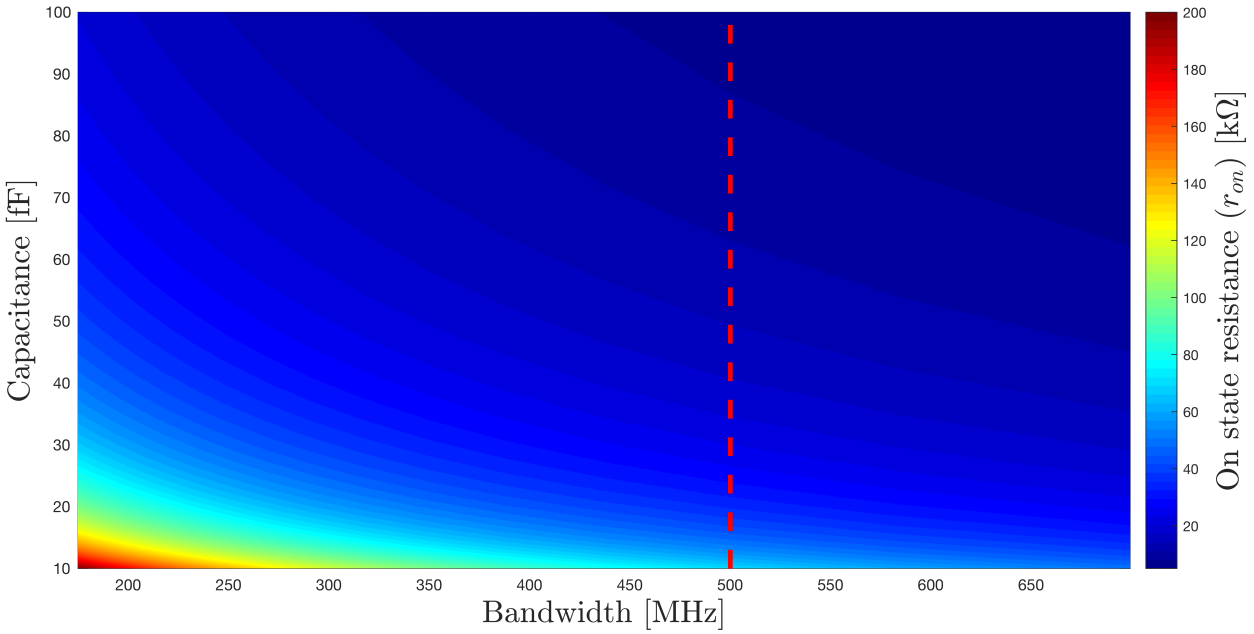
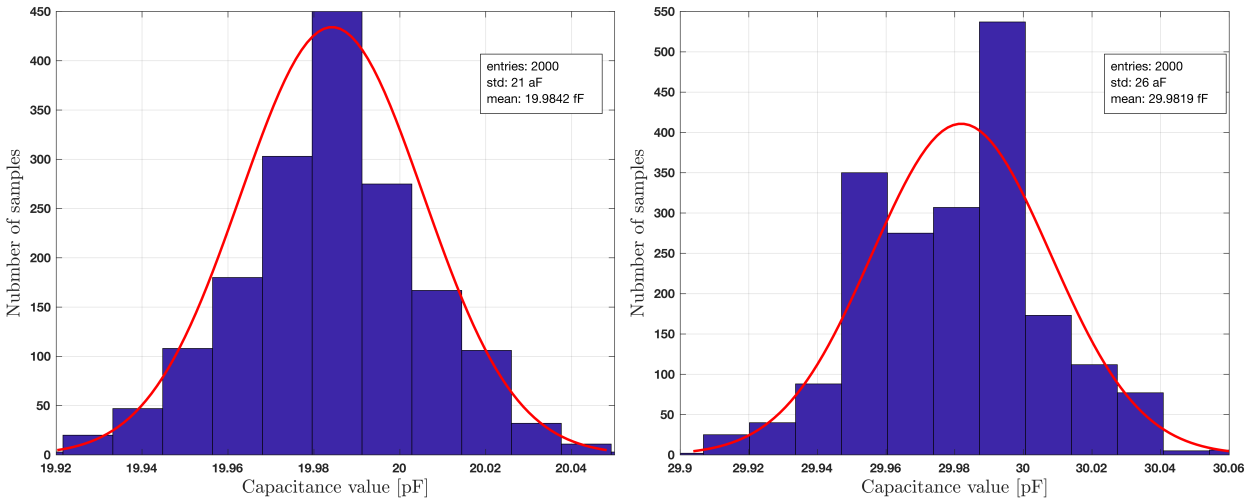


Figure 4.5: On-state resistance as a function of capacitance and bandwidth.

From both analyses, the optimal capacitor value for this design is 30 fF. Figures 4.6a and 4.6b show the distribution of the sampling capacitance using the mismatch models provided by TSMC. The Monte Carlo simulation for 20 fF and 30 fF capacitance values for metal-insulator-metal (MIM) capacitors shows a negligible standard deviation. These simulations were performed in order to evaluate if the manufacturing process variations will effect the performance of the system. It has to be noted that the transmission gate will introduce parasitic capacitance, thus noticeably increasing the overall sampling capacitance.

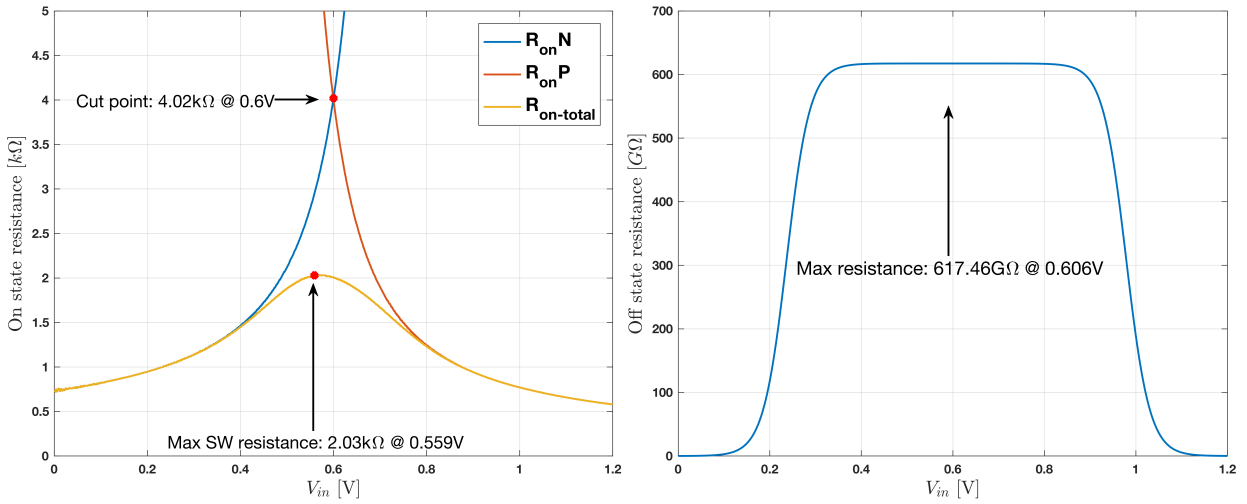
The transmission gate was optimized to have low enough on-state resistance to provide the necessary bandwidth and at the same time have as low resistance variance as possible. From the analysis shown in Figure 4.5, the on-state resistance should not exceed 20 kΩ range. However, due to space constraints it has been decided that the switch dimensions should be kept as small as possible while maintaining the performance.

By experimenting with the switch dimensions, it was found that designing for an on-state resistance below 2 kΩ makes the switch response very non-linear over the input voltage range and is thus not a practical solution. The simulation results of the on-state resistance for both, NMOS and PMOS transistors, and the total on-state and off-state resistances of the switch as a function of input voltage are shown in Figures 4.7a and 4.7b, respectively.



(a) (b)

Figure 4.6: (a) Monte Carlo process variation simulation for 20fF MIM Capacitor. (b) Monte Carlo process variation simulation for 30fF MIM Capacitor.



(a) (b)

Figure 4.7: (a) Transmission gate on-state resistance as a function of input voltage. (b) Transmission gate off-state resistance as a function of input voltage.

After designing the transmission gate to have the desired operation, the total capacitance of the sampling cell was evaluated to estimate the contribution of the parasitic capacitance; the result is shown in Figure 4.8.

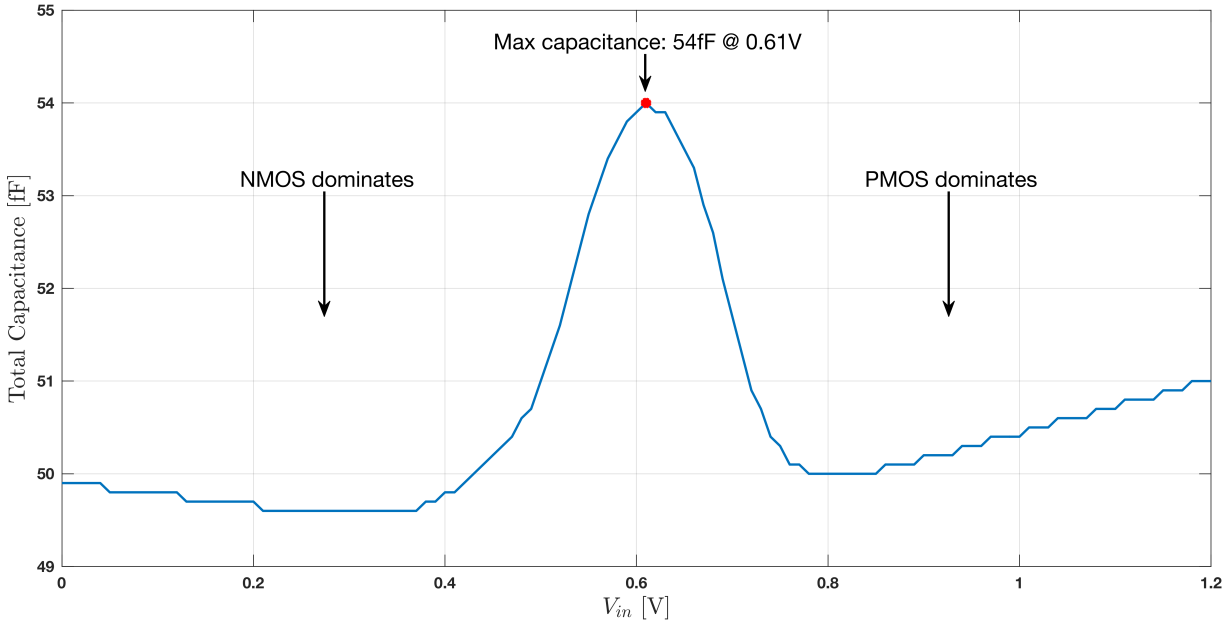


Figure 4.8: Total capacitance of the transmission gate and sampling capacitor as a function of input voltage.

The total capacitance of the sampling cell increases up to 24 fF due to the parasitic capacitance from the switch; the capacitance is highest when both transistors are in transition. By using the Equation 4.2, the maximum acceptable on-state resistance for this capacitance can be found to be approximately 6 kΩ, which satisfies the BW requirement, thus extra precautions are not required [12].

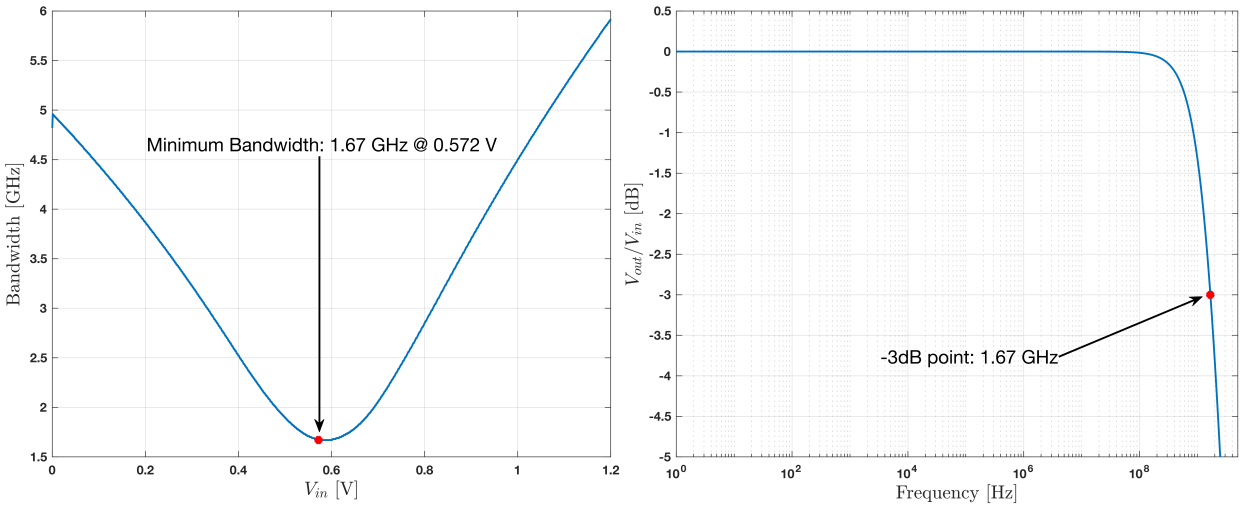
$$f_{-3dB} = \frac{1}{2\pi RC} \tag{4.2}$$

After characterizing the capacitance of the sampling cell and designing the switch, the BW of the sampling cell was thoroughly evaluated. The BW as a function of input voltage is shown in Figure 4.9a, while Figure 4.9b shows the frequency response in terms of magnitude at the point of worst case BW.

As stated before the leakage current is a potential issue in sampling cell. Thus, a several scenarios have been evaluated:

1. The capacitor is fully charged, switch is opened and the voltage is pulled to ground; results are shown in Figure 4.10a.

2. The capacitor is charged to 1 V and the voltage is dropped to 0.4 V; results are shown in Figure 4.10b.

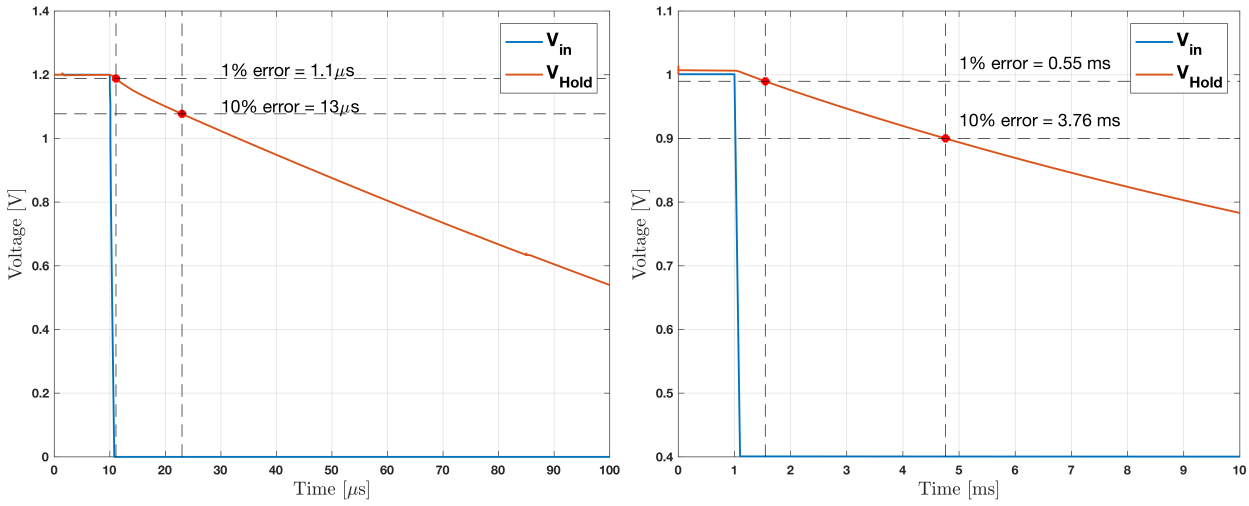


(a) (b)

Figure 4.9: (a) Bandwidth of the full sampling cell as a function of input voltage. (b) Worst case bandwidth of the full sampling cell.

When the voltage on the input side of the switch drops, the capacitor starts to discharge through the transmission gate off-state resistance. The effect of the leakage current is highest near the power supply rails; more specifically, the isolation of NMOS transistor drops near VDD. On the other side of the voltage range the same holds true for the PMOS. This is due to sub-threshold conduction, where a weak inversion layer still exists on the channel and thus some current flows from the drain to the source, even though the transistor should be completely closed [13]. This effect can be seen in Figure 4.7b, which shows the non-linear off-state resistance of the transmission gate. The switch performs best around mid-range (VDD/2), where both of the transistors are in transition. Figure 4.10a shows the worst case scenario where the leakage current leads to a 1 % error of the sampled voltage after only 1.1 µs.

The sampling cell layout is shown in Figure 4.11. The layout can drastically affect the device operation due to the parasitic capacitance and resistance introduced by the traces and other layout structures. Thus, after finishing the layout, the same simulations were repeated with the extracted parasitic elements from the layout to see the effects on the overall performance. The post-layout simulation results are shown in Figures 4.12, 4.13, and 4.14 and the comparison of the simulation results are summarized in Table 4.2.



(a) (b)

Figure 4.10: (a) Leakage current as the voltage is dropped from 1.2 V to 0 V. (b) Leakage current as the voltage is dropped from 1 V to 0.4 V.

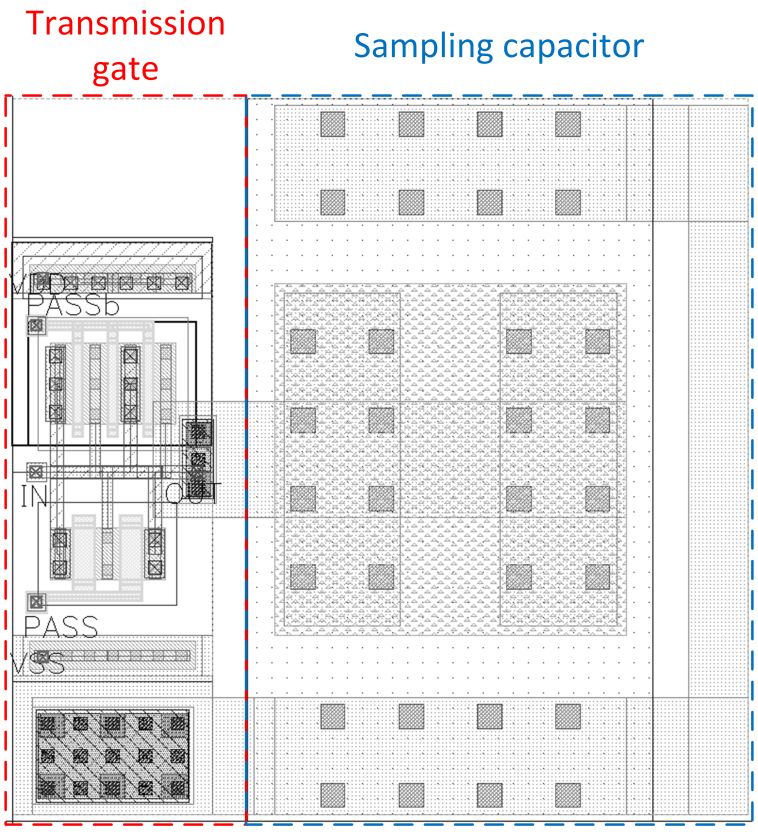
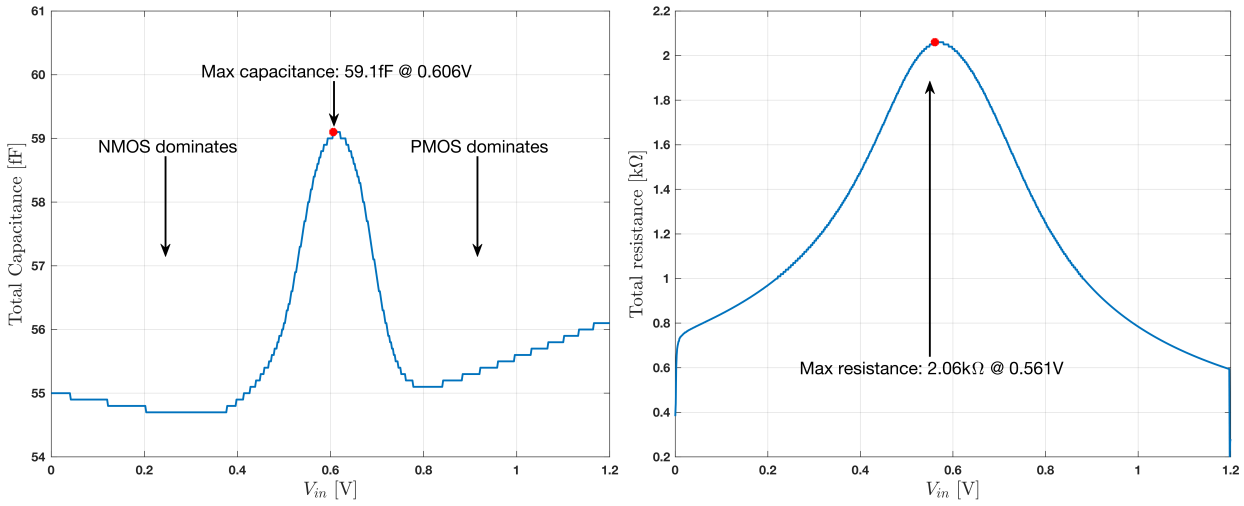
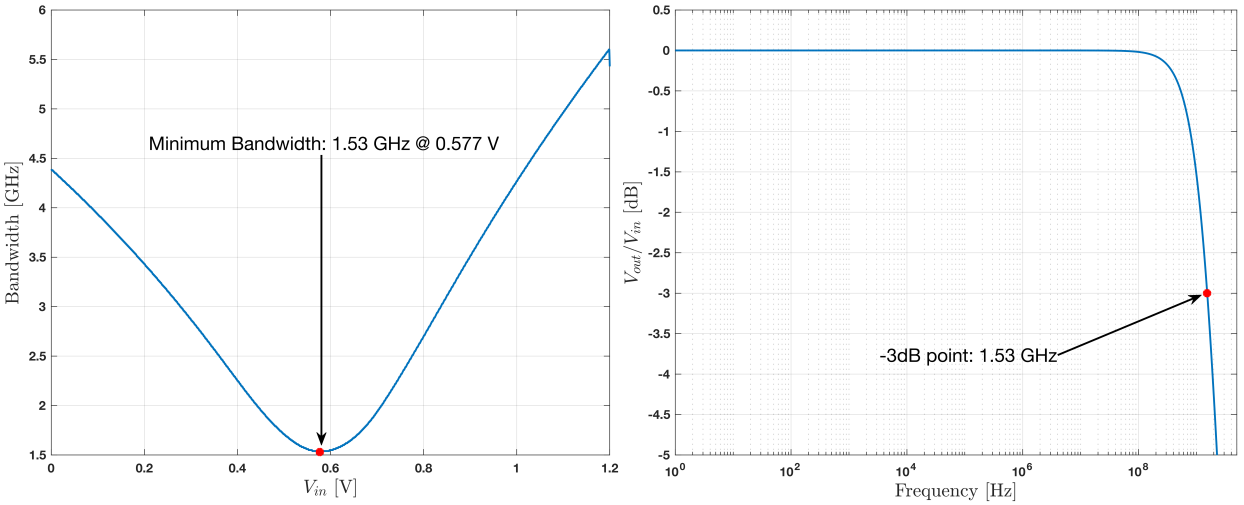


Figure 4.11: Sampling cell Layout.



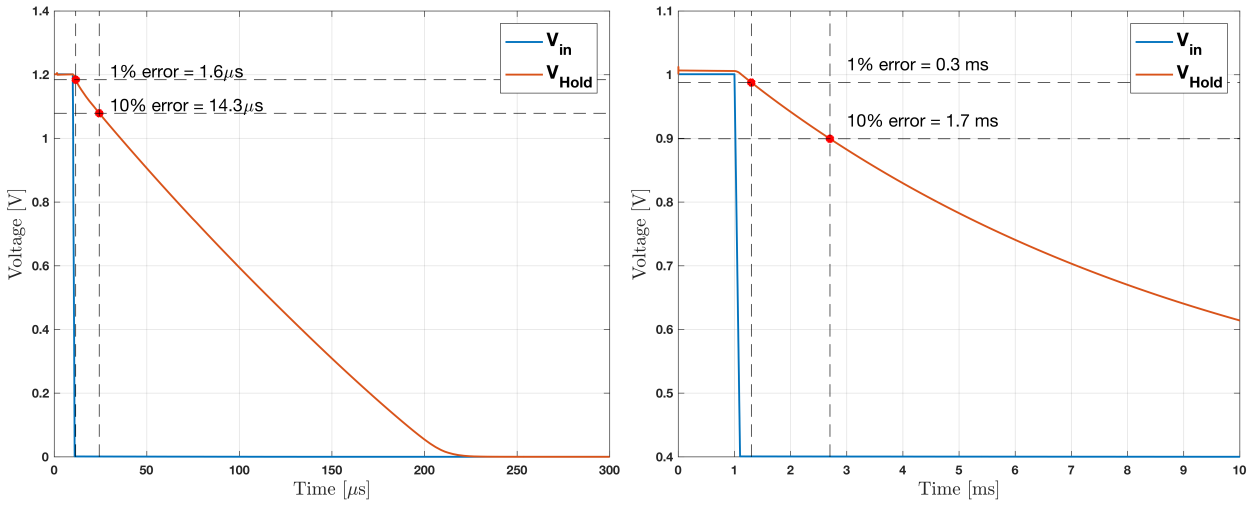
(a) (b)

Figure 4.12: (a) Total capacitance of one sampling cell as a function of input voltage with parasitic extraction. (b) Total transmission gate resistance as a function input voltage with parasitic extraction.



(a) (b)

Figure 4.13: (a) Bandwidth as a function of input voltage with parasitic extraction. (b) Worst case bode plot with parasitic extraction.



(a) (b)

Figure 4.14: (a) Leakage current as the voltage is dropped from 1.2 V to 0 V with parasitic extraction. (b) Leakage current as the voltage is dropped from 1 V to 0.4 V with parasitic extraction.

Table 4.2: Sampling cell comparison of pre-layout and post-layout simulation results.

	Pre-layout	Post-layout
Maximum on-state resistance	2.03 kΩ	2.06 kΩ
Maximum capacitance	54 fF	59.1 fF
Minimum bandwidth	1.67 GHz	1.53 GHz
1% leakage error - 1.2 V ⇒ 0 V	1.1 µs	1.6 µs
10% leakage error - 1.2 V ⇒ 0 V	13 µs	14.3 µs
1% leakage error - 1 V ⇒ 0.4 V	550 µs	300 µs
10% leakage error - 1 V ⇒ 0.4 V	3.76 ms	1.7 ms

4.1.2 Comparator

The GRAPH sampling unit comparator is composed of three stages:

1. The input stage, made up of two complementary differential pair.
2. The gain stage, which is a push-pull amplifier.
3. The output stage, which is a basic inverter circuit design to operate in the class AB amplifier regime.

In order to meet the initial design requirements in terms of low power consumption and low material budget, while maintaining the necessary performance, the comparator was optimized for

driving one first in, first out (FIFO) register; more specifically the FIFO register consists of 12 DFFs, representing a load capacitance of 26.1 fF. In addition, the comparator needs to operate from rail to rail in order to preserve the signal headroom. Its specifications are listed in Table 4.3.

Table 4.3: Comparator specifications.

	Specification
Input common mode range	0 V ⇒ 1.2 V
Output dynamic range	0.1 V ⇒ 1.1 V
Maximum current consumption	10 µA
Minimum load drive capability	> 26.1 fF load

The rail-to-rail input common mode operation is very important in this design due to the limited voltage headroom (1.2 V) of the 130 nm CMOS process. In order to meet this requirement, the comparator takes advantage of a complementary differential pair design as shown in Figure 4.15 [4]. When one of the pairs is off the other is on and vice versa, thus ensuring a rail-to-rail input common-mode voltage range.

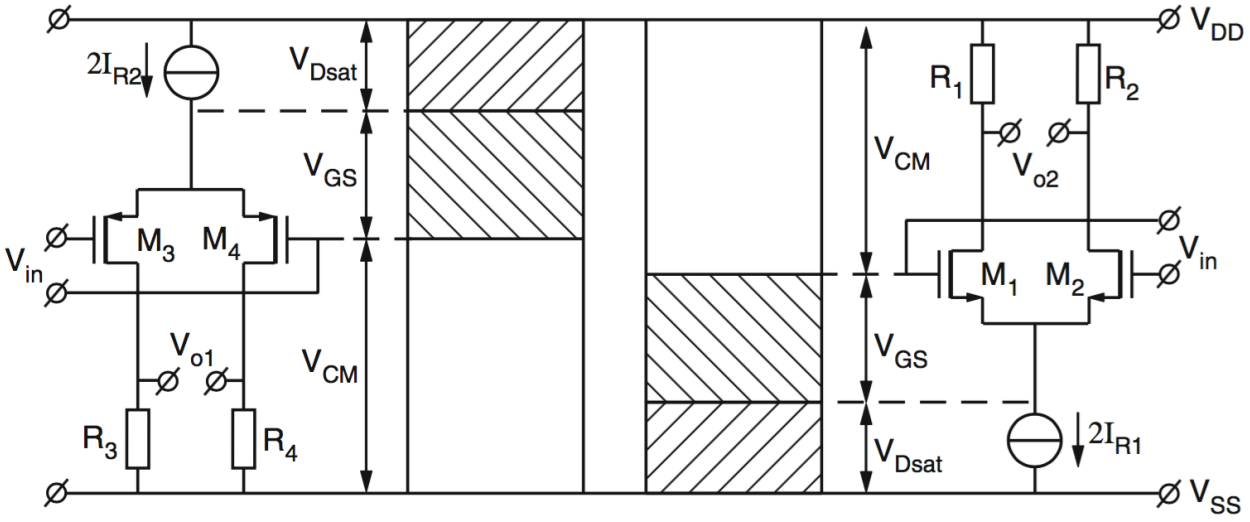


Figure 4.15: Common-mode input voltage range of a PMOS and an NMOS input stages [4].

In order to conserve power, the input stage is driving a push-pull gain stage. Its topology consists of a series combination of NMOS and PMOS transistors, where the NMOS differential pair output controls the PMOS transistor and the PMOS differential pair output controls the NMOS transistor. In this way, when the comparator is not active, the current flow from the push-pull stage is reduced to minimum, thus reducing the static power consumption.

The gain stage is driving a class AB amplifier, consisting of a basic inverter circuit, which draws only a minimal amount of current when not in use and has the adequate strength to drive the load when in operation. The schematic view along with the corresponding layout are shown in Figures 4.16a and 4.16b, respectively.

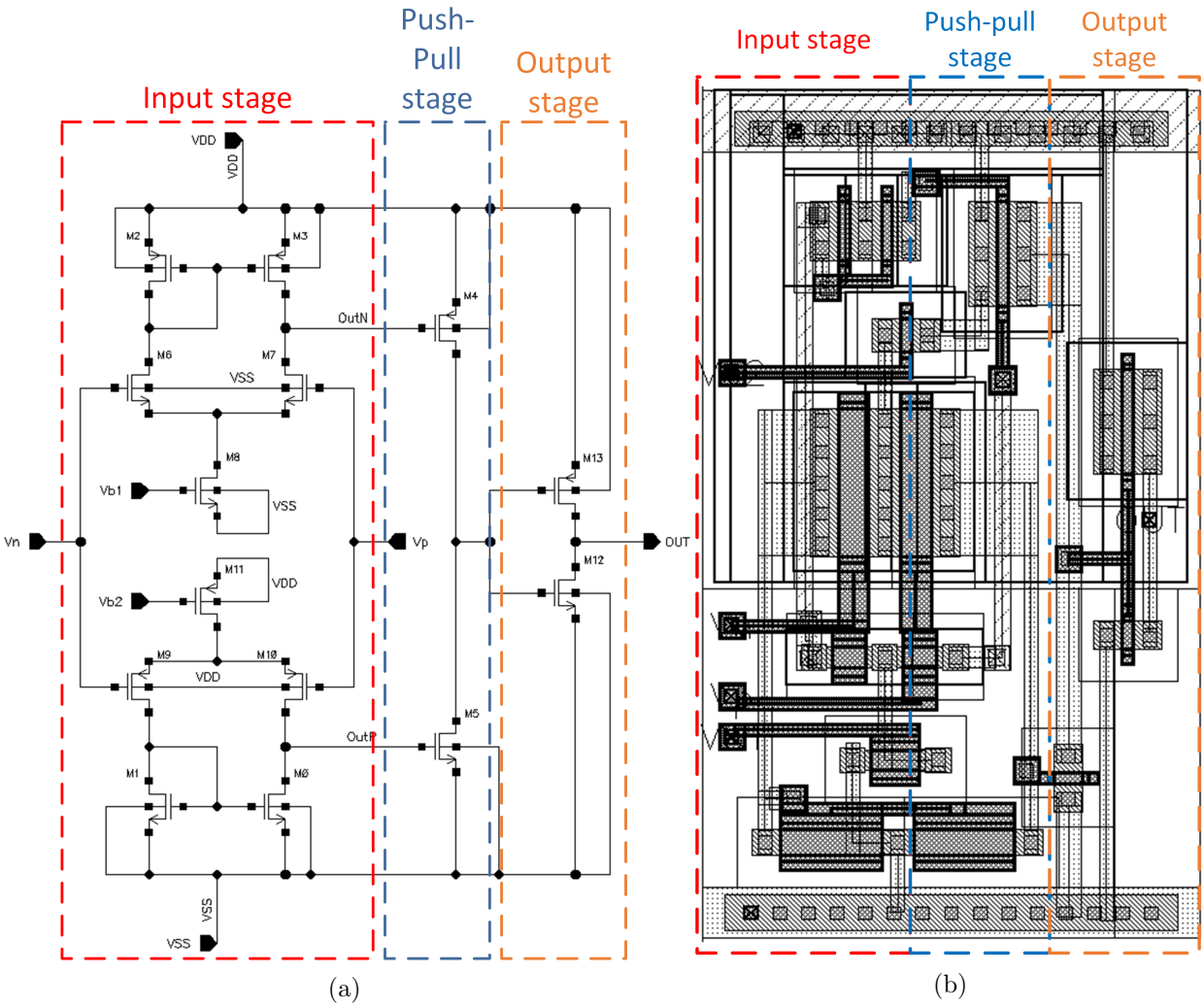
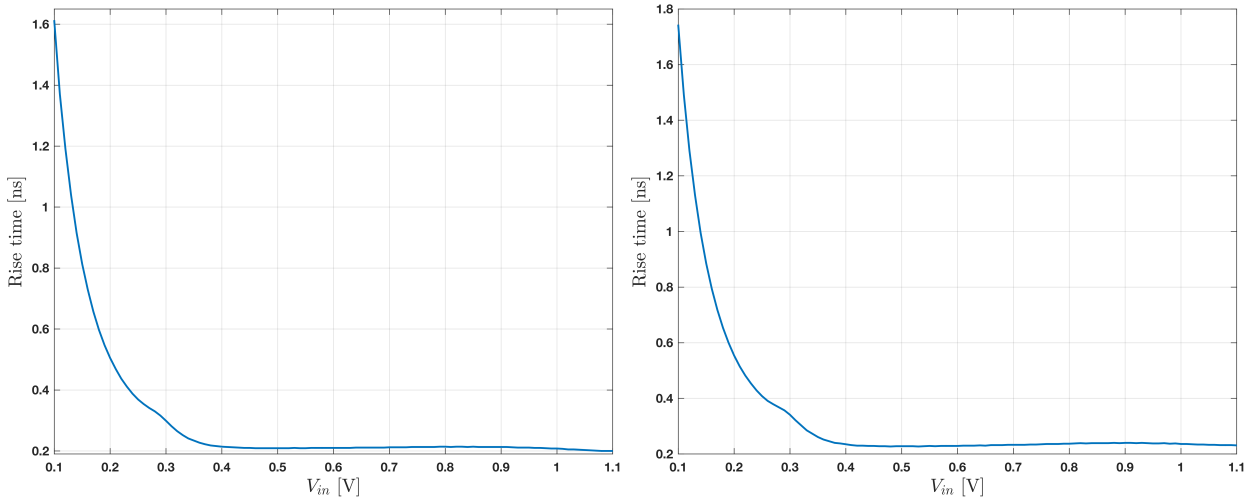


Figure 4.16: (a) GRAPH ASIC comparator schematic. (b) GRAPH ASIC comparator layout.

The comparator performance was characterized for both, pre-layout and post-layout cases in terms of rise time, fall time, and propagation delay. In the case of pre-layout simulations, the results are shown in Figures 4.17a, 4.18a, and 4.19a. Likewise, the post-layout simulation results are shown in Figures 4.17b, 4.18b, and 4.19b.

Figure 4.17 shows a plot of the rise time as a function of input voltage for the pre-layout and post-layout cases. The rise time is relatively constant from 0.2 V to 1 V. Below 0.2 V the rise time increases drastically, which directly impacts to both propagation delay and the output linearity of

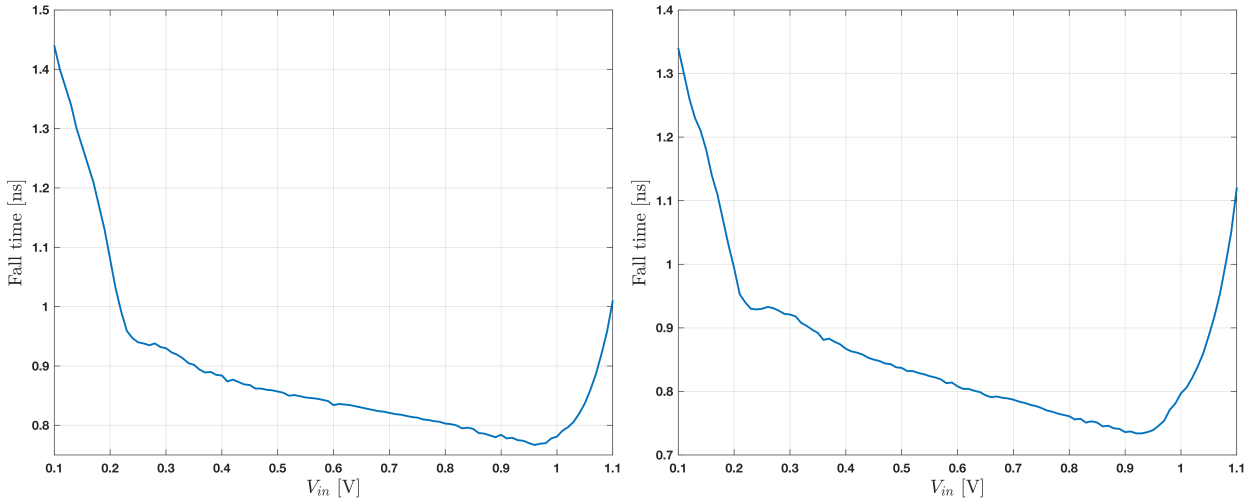
the Wilkinson ADC.



(a) (b)

Figure 4.17: (a) Comparator rise time as a function of input voltage (pre-layout case). (b) Comparator rise time as a function of input voltage (post-layout case).

The only requirement for the comparator fall time is to be faster than the ramp generator reset time, which is approximately 30 ns. As seen in Figure 4.18, the fall time for this design is less than 2 ns, thus satisfying the requirement.

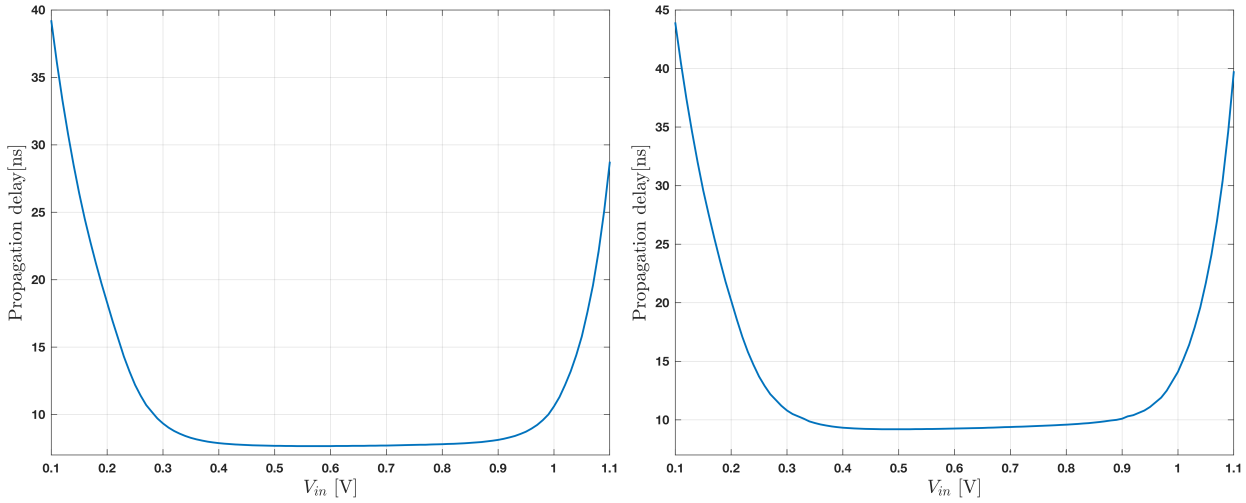


(a) (b)

Figure 4.18: (a) Comparator fall time as a function of input voltage (pre-layout case). (b) Comparator fall time as a function of input voltage (pre-layout case).

In Wilkinson type ADCs the propagation delay of the comparator directly affects the output

linearity of the converter. That is, a variable propagation delay leads to a variable offset in ADC counts, thus introducing distortion and making the calibration procedure more complex. Figure 4.19 shows a relatively constant propagation delay between 0.2 V to 1 V. If further linearity is needed, the comparator could be further improved to make the propagation delay constant over a wider range of voltages. However, this would directly impact the current consumption of the comparator, which is not desirable.



(a) (b)

Figure 4.19: (a) Comparator propagation delay as a function of threshold voltage. (b) Comparator propagation delay as a function of threshold voltage after parasitic extraction.

Another important constraint of the comparator is the power consumption, more specifically the comparator current draw should not exceed 10 µA. The current draw as a function of the input voltage is shown in Figure 4.20. The current draw does not exceed 6 µA and thus satisfies this requirement.

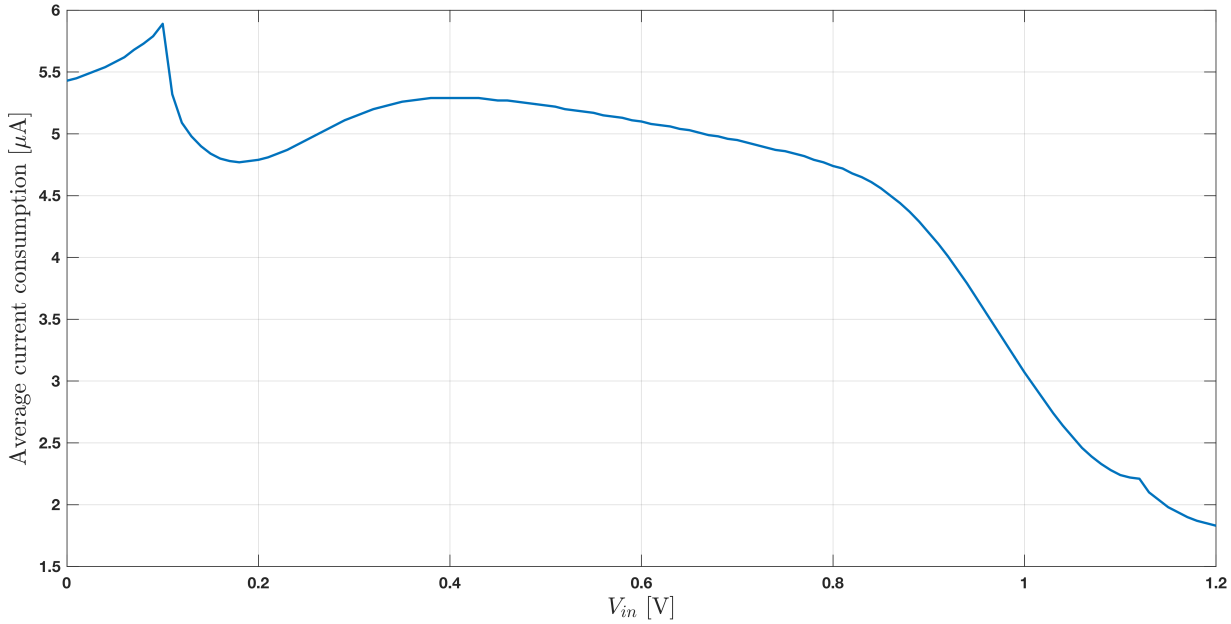


Figure 4.20: Average current consumption of the comparator as a function of the threshold voltage.

After characterizing the comparator, its performance was evaluated with the test setup shown in Figure 4.21. The test was performed by following the steps, listed below:

1. The input threshold voltage was set to 0.6 V for the inverting input of the comparator.
2. A 1 µs ramp voltage from 0 V to 1.1 V was applied to the non-inverted input.
3. The output of the comparator was simulated. The transient results can be seen in Figure 4.22a.

The slew rate simulation is shown in Figure 4.22b and the extrapolated slew rate is 1620 $\frac{\text{V}}{\mu\text{s}}$.

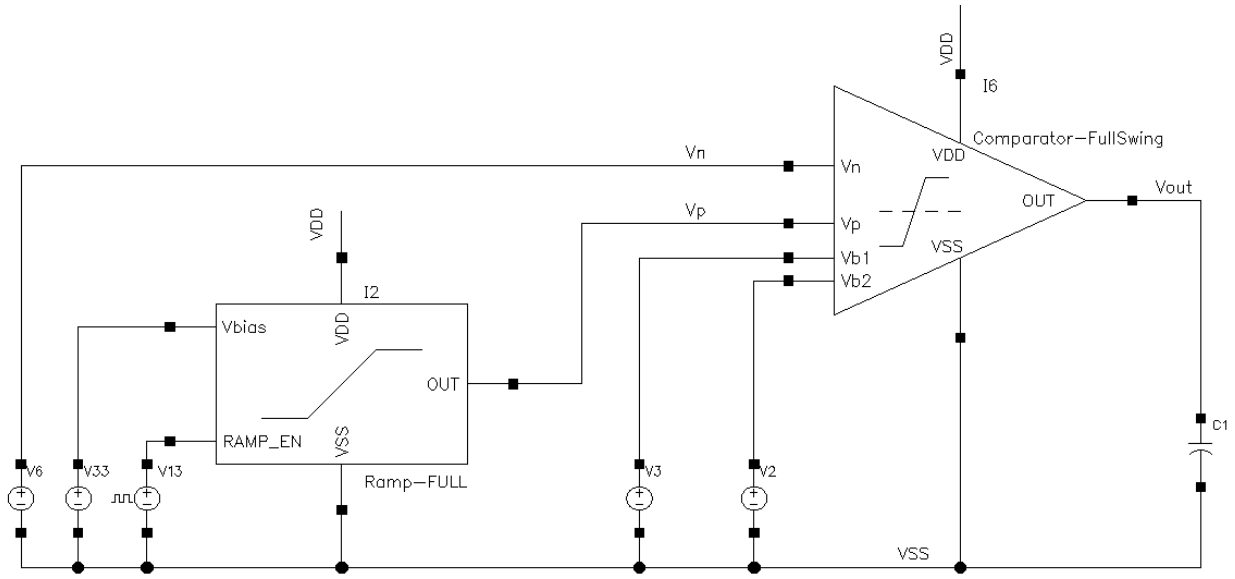
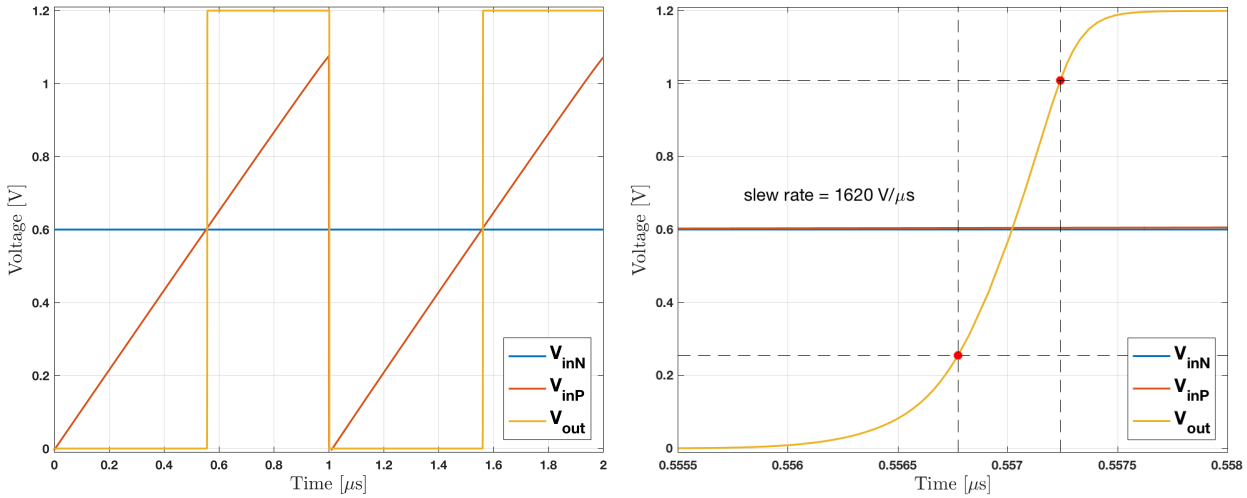


Figure 4.21: Comparator test setup.



(a) (b)

Figure 4.22: (a) Transient simulation of the comparator. (b) Slew rate of the comparator, extracted from the transient simulation.

4.1.3 Ramp generator

The ramp generator has been designed to provide the linear voltage ramp for the Wilkinson ADC. The requirements for the ramp generator are: linear range from 0.1 V to 1.1 V; 1 µs ramp time; ramp time and sequence needs to be programmable.

A linear voltage ramp can be achieved by charging a capacitor with a constant DC current from a current source. The ramp sequence control is performed by using one NMOS transistor, functioning as a switch. The schematic of the ramp generator is shown in Figure 4.23.

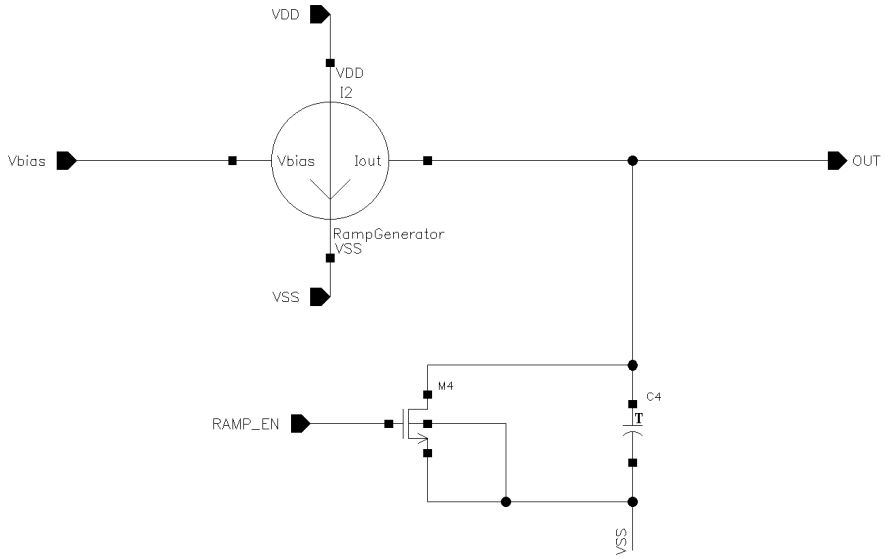


Figure 4.23: Schematic of the ramp generator.

As the current flows into the capacitor, a constant ramp is generated as Equations 4.3, 4.4, and 4.5 indicates.

$$\frac{dq(t)}{dt} = C \times \frac{dV_{out}}{dt} \tag{4.3}$$

$$I(t) = C \times \frac{dV_{out}}{dt} \tag{4.4}$$

$$V_{out} = V_{out}(0) + \frac{1}{C}\int_0^t I(t)dt \tag{4.5}$$

The current source must be designed to maintain a constant output current under large voltage swings. That is, it must have large output impedance. The ramp voltage is generated by integrating the current source current on a capacitor. In order to have a linear voltage ramp, the current has to remain constant and thus the current source must remain in saturation. Eventually the voltage will be too large for the current source to maintain saturation, thus leading the current source into a non-linear operation; this effect is called channel length modulation, which is one of the fundamental second order effects in CMOS circuit design [13].

There are many different topologies for CMOS current sources, each with their own benefits. Since the ramp generator voltage changes from 0 to 1.2V and the maximum linear range is desired,

a "high swing cascode" current source topology was chosen; the schematic view of the current source is shown in Figure 4.24a. A benefit of this topology is that it has large output impedance and it can remain constant under large voltage swings. The Figure 4.24b presents the I-V curve for the high swing cascode current source. As the graph shows, this topology remains reasonably linear in saturation region. However, this topology can only provide small amount of output current unless very large transistor structures are used. This would increase the device capacitance, leading to a poorly defined output capacitance of the ramp generator. The simulated performance for this current source topology driving a 1 pF capacitor and providing a voltage ramp is presented in Figure 4.25 [13].

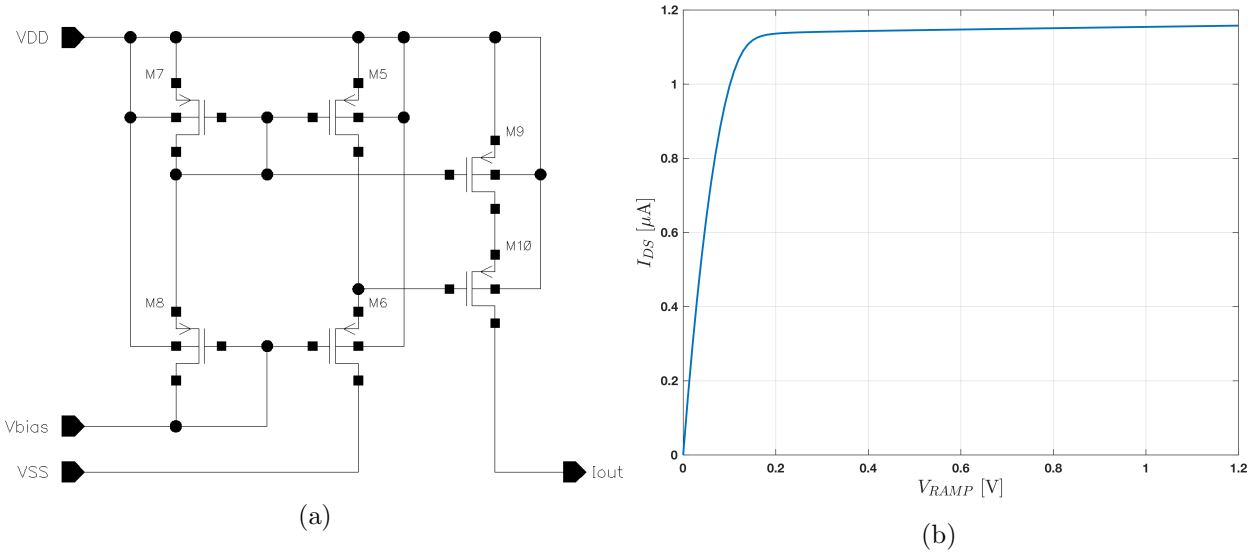
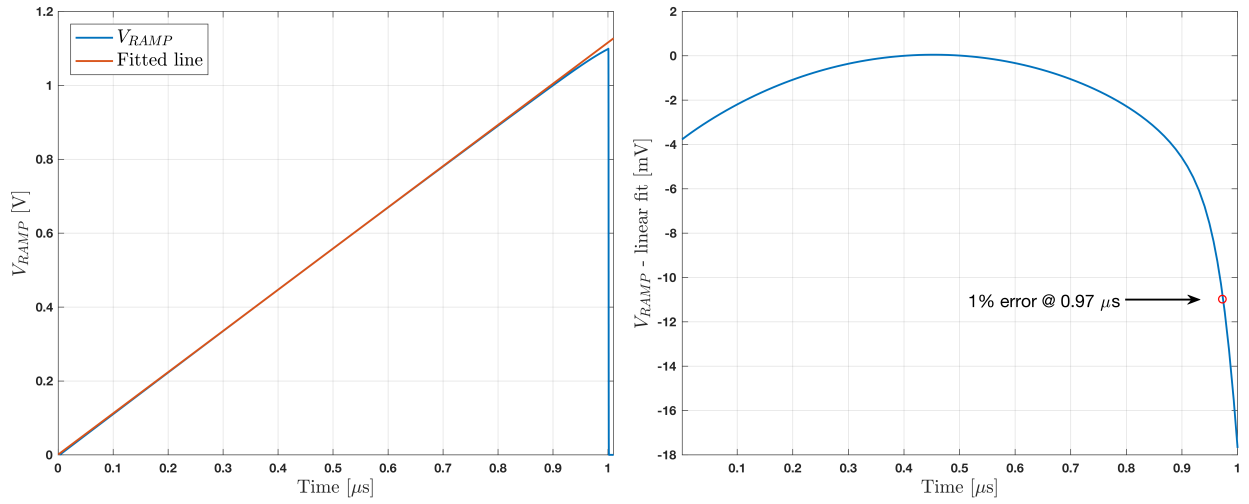


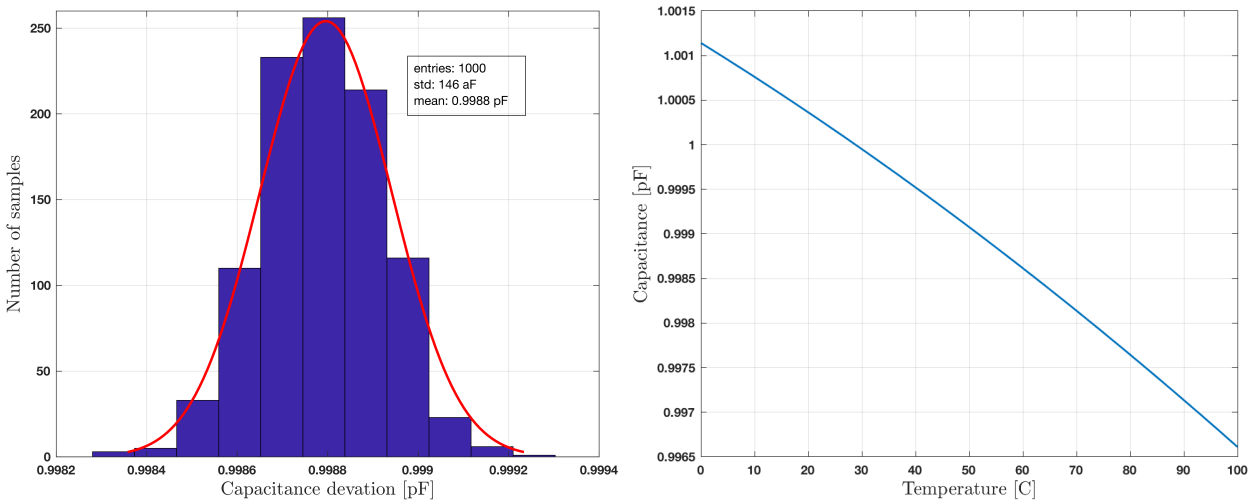
Figure 4.24: (a) Schematic view of the high swing cascode current source. (b) I-V curve of the high swing cascode current source.

As the Figures 4.25a and 4.25b illustrates, the linearity of the ramp is acceptable over the desired range; the non-linearity error is less than 2% for the full range from 0 V to 1.1V. However, it has to be noted that there are other sources that may contribute to the non-linear response of the ramp. Some of them are temperature and process variations. Figures 4.26a and 4.26b temperature and process variations effect on the ramp generator capacitance.



(a) (b)

Figure 4.25: (a) Voltage ramp as a function of time. Red line denotes the linear fit for the ramp. (b) Relative error of the ramp as a function of time-varying input voltage.



(a) (b)

Figure 4.26: (a) Monte Carlo process variation mismatch simulation results for the capacitor used for ramp generator. (b) Capacitor value drift as a function of temperature.

In conclusion, the temperature and the process variations only minimally effect the design. However, the ramp time can be calibrated for these variations. Figure 4.27 shows the current source output current as a function of bias voltage. By tuning this voltage, the net effect of temperature and process variations can be mitigated.

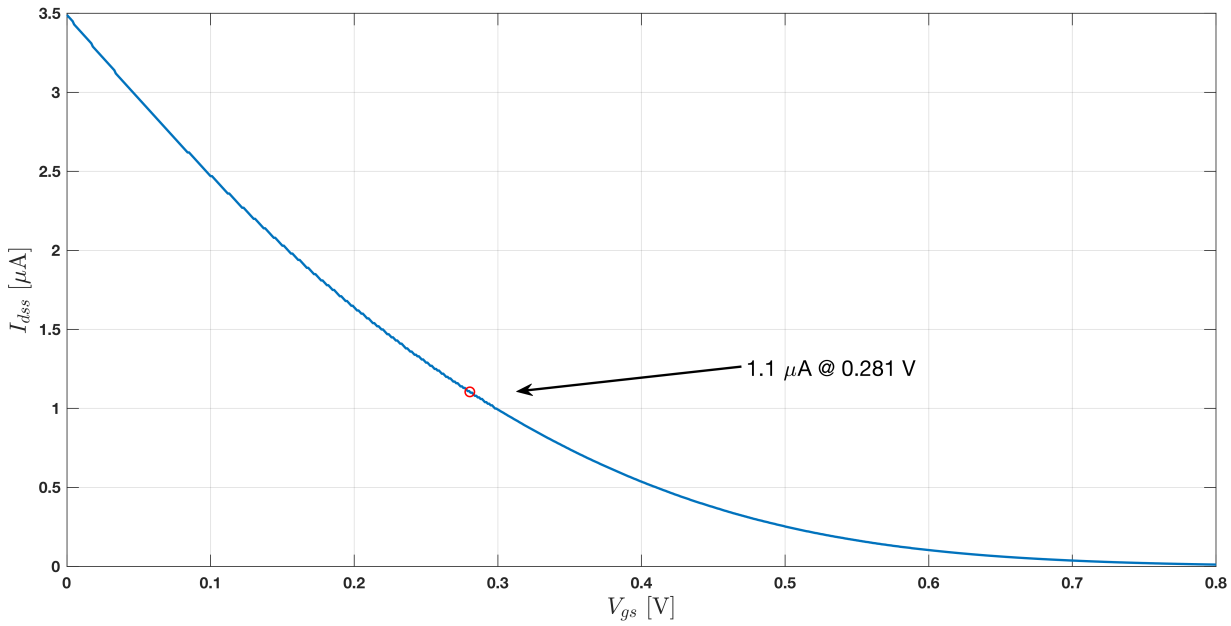
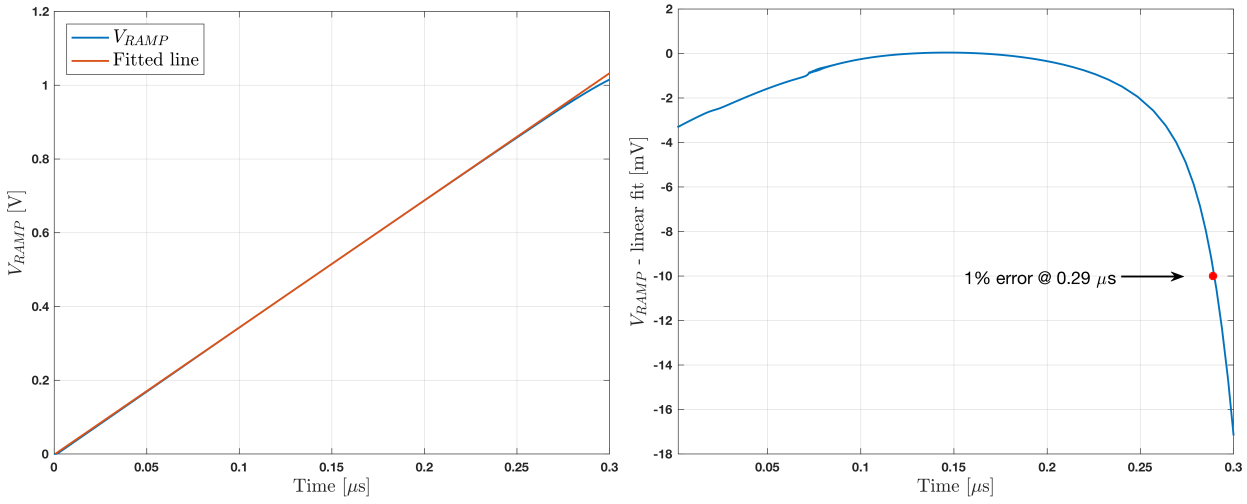


Figure 4.27: Current source current as a function of bias voltage.

As Figure 4.27 illustrates, the controlling range is very large. In Figures 4.28a and 4.28b it can be observed that the ramp operates very well even at the limits of the current source operation. However, it should be noted that since the transistor threshold voltages vary as a function of gate-to-source voltage (V_{GS}), the voltage headroom is limited for faster ramps.



(a) (b)

Figure 4.28: (a) Ramp generator output voltage as a function of time for higher current. (b) Relative error of the ramp as a function of time varying input voltage for higher current.

After the compelete characterization, the layout of the ramp generator was designed as shown in Figure 4.29 and the post-layout simulation performed; the results are shown in Figures 4.30a and 4.30b. In addition, the performance of the pre-layout and post-layout simulations is summarized in Table 4.4.

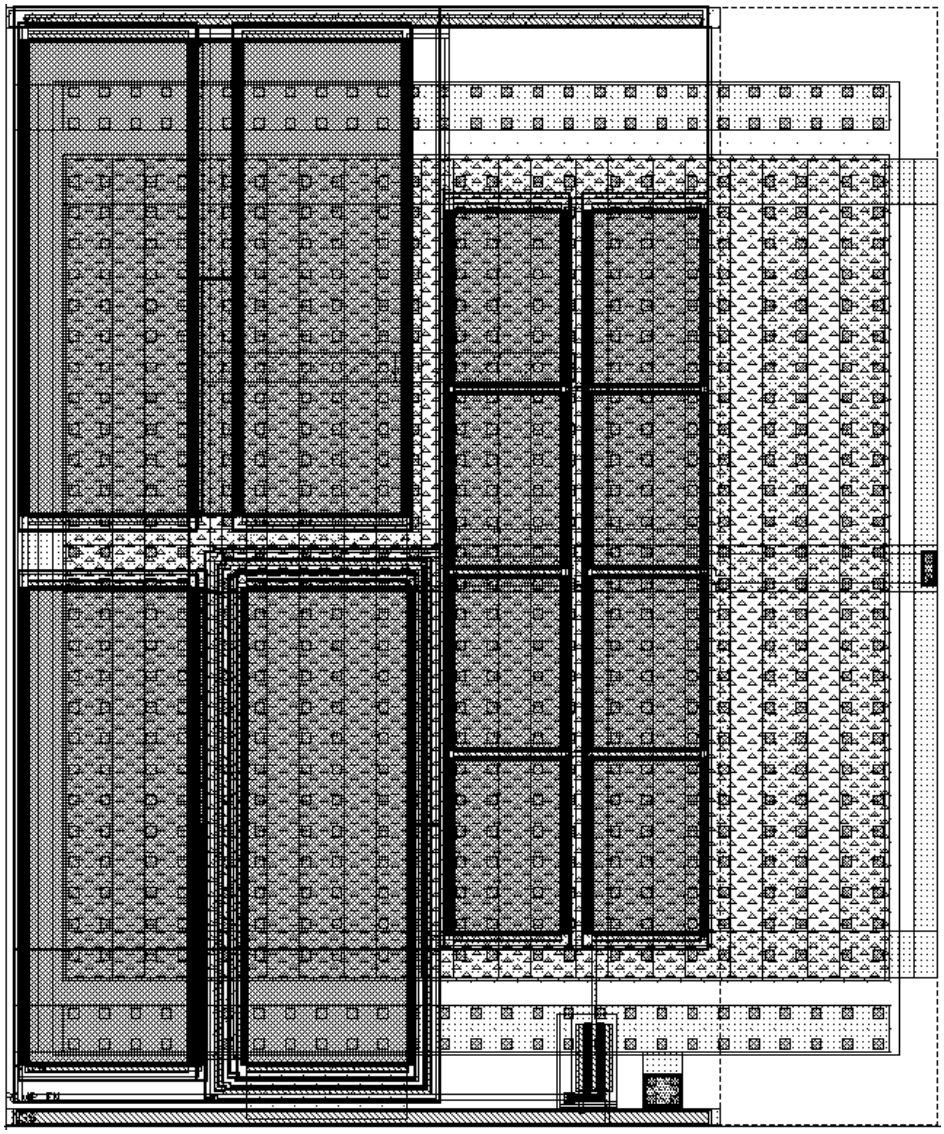
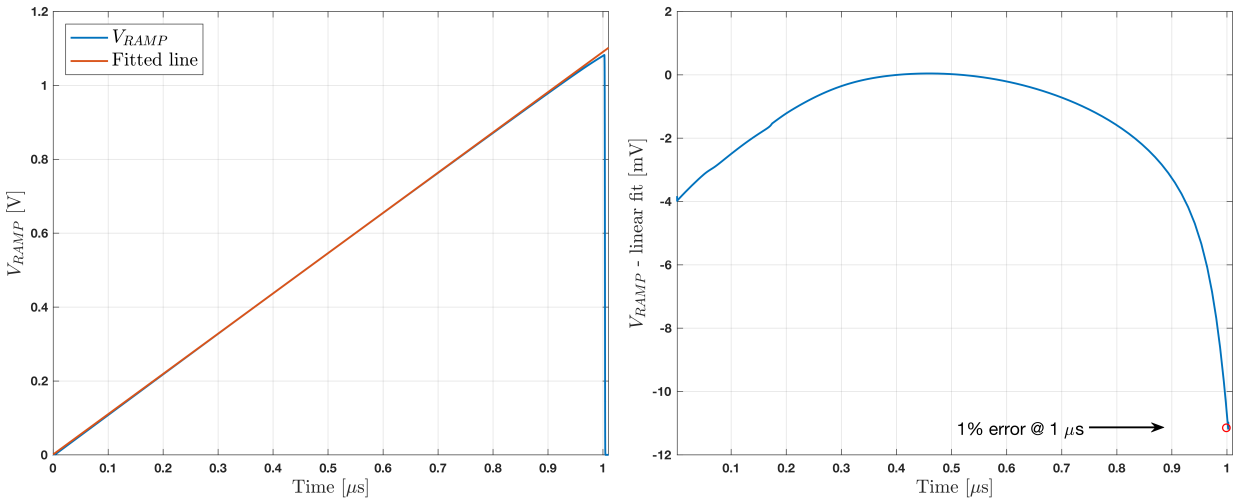


Figure 4.29: Ramp generator layout.



(a) (b)

Figure 4.30: (a) Voltage ramp as a function of time. Red line denotes the linear fit for the ramp. (b) Relative error of the ramp as a function of time-varying input voltage.

Table 4.4: Ramp generator - a comparison of the simulation results.

	Pre-layout	Post-layout	Fast ramp
Linear range	0V ⇒ 1.1 V	0V ⇒ 1.1 V	0V ⇒ 1.02 V
1 % error	0.97 µs	1 µs	300 ns
Ramp time	1 µs	1 µs	300 ns

4.1.4 Buffer amplifier for ramp generator

A buffer amplifier (OTA) has been designed in order to isolate the ramp generator from the capacitive load of 64 comparator inputs, thus maintaining the ramp generator performance. The full load capacitance of the 64 comparator inputs has been found to be 275 fF. It has to be noted that this capacitance slightly deviates as a function of input voltage and the reported value represents its worst assessment. Even if the ramp generator would have been able to drive a constant current into this load, the output would be very non-linear without the active feedback component due to the deviating load. The buffer has five stages as shown in Figure 4.31:

1. Biasing stage, for setting the operating point.
2. Input stage, which is made up of two complementary differential pairs to achieve input common mode rail-to-rail operation [4] [14].

3. Cascode gain stage, which increases the output impedance and transconductance of the amplifier, thus adding gain [13].

4. Output stage, which is a basic inverter circuit that is designed to operate as a class AB amplifier.

5. Miller compensation circuit, which is designed to provide enough separation of the poles introduced by the cascode and output stages to stabilize the frequency response of the amplifier [13].

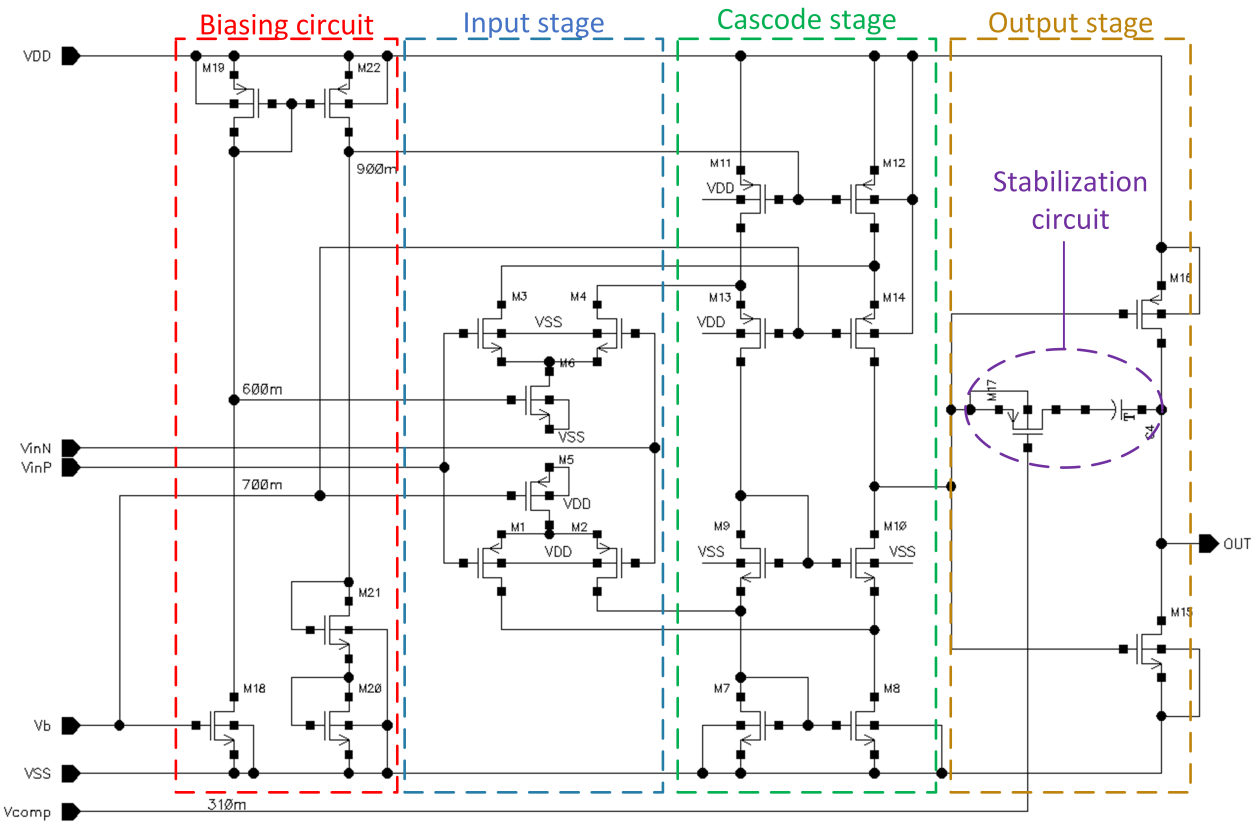


Figure 4.31: Schematic of the buffer for ramp generator.

The performance of the OTA was evaluated through simulation of various performance parameters. First its low signal BW and phase margin were evaluated by performing an AC analysis. The results are shown in Figure 4.32. As the result shows, with a phase margin of 67 degrees the amplifier has a very stable response over the BW, which is approximately 117 MHz.

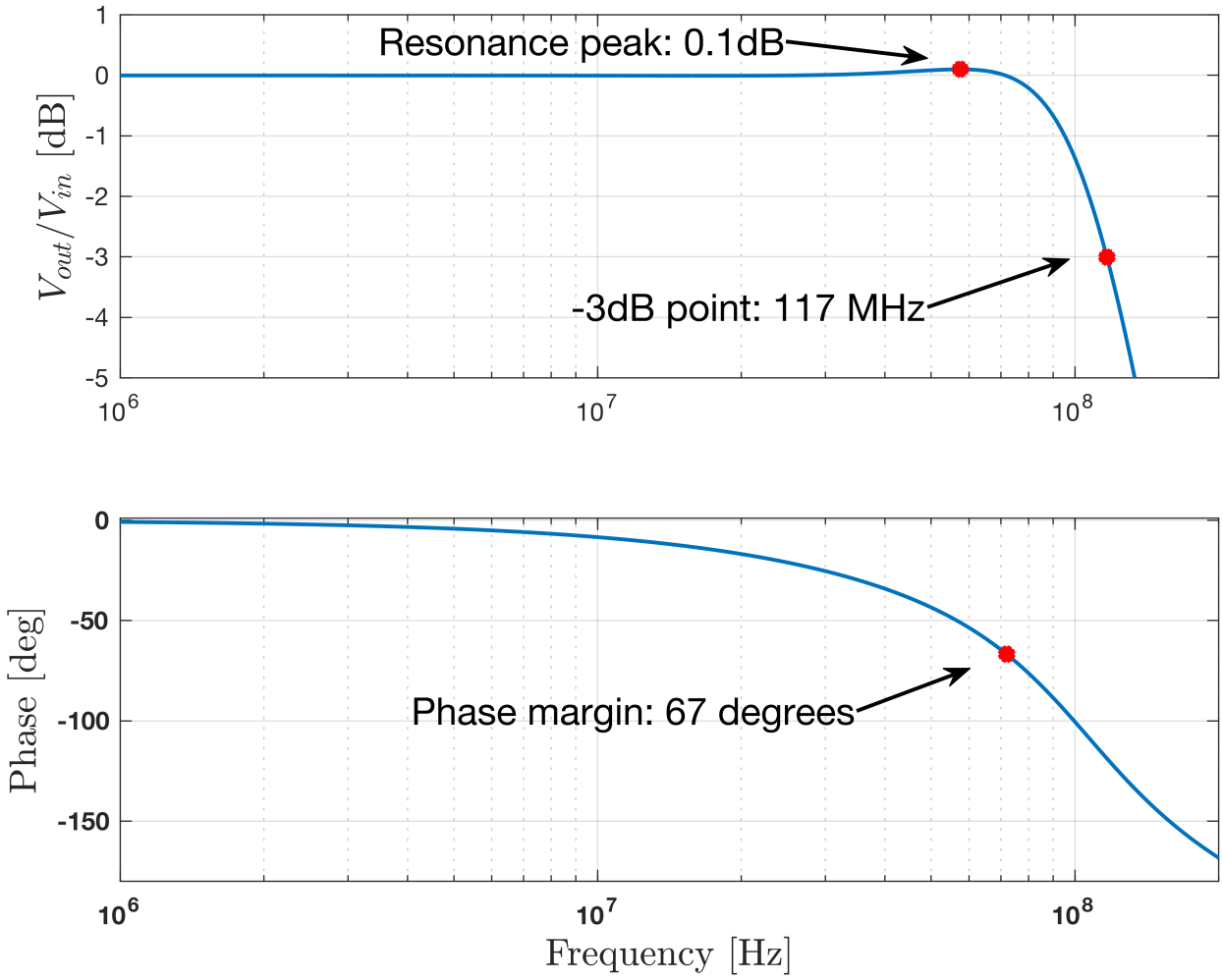
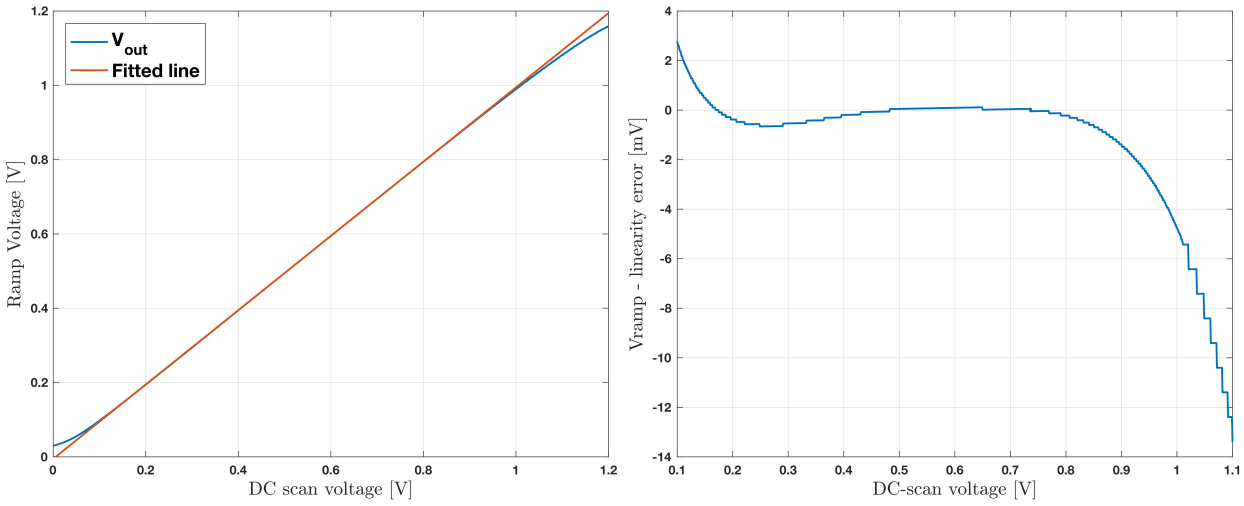


Figure 4.32: Buffer amplifier bandwidth and phase margin.

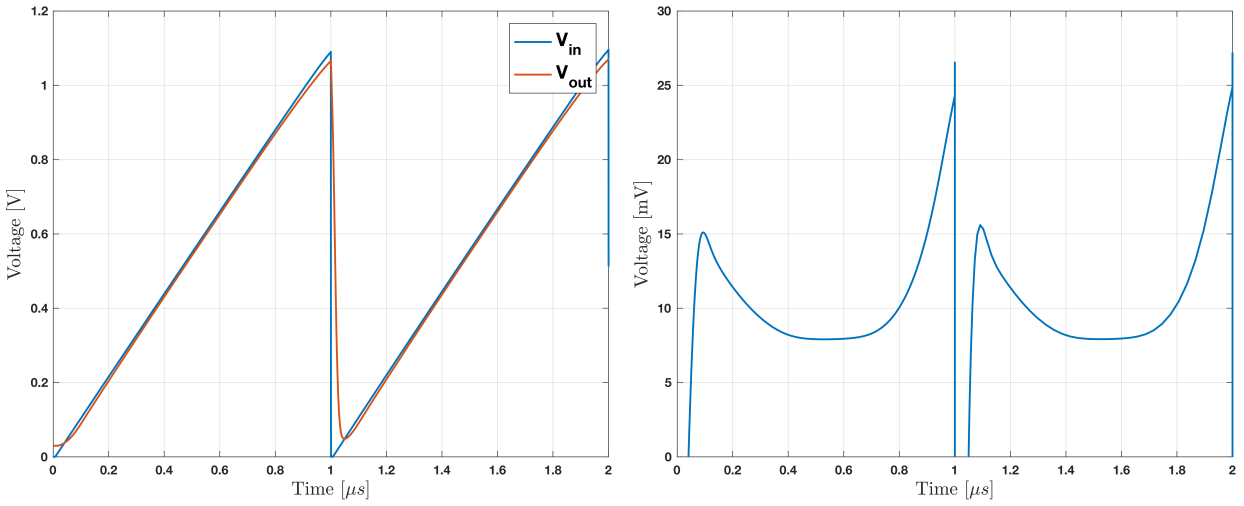
Second, the linearity of the amplifier was evaluated by performing a DC scan from 0 V to 1.2 V with 1 mV steps and comparing how the output matches the input. The linearity result are shown in Figures 4.33a and 4.33b. As the simulation illustrates, the buffer is very linear over the desired dynamic range (0.1 V to 1.1 V), where the maximum error is approximately 1.4 %.



(a) (b)

Figure 4.33: (a) The buffer output as a function of the input voltage. (b) Relative error of the buffer as a function of the input voltage.

Third, the buffer was tested with the ramp generator in transient simulation. The transient simulation results are shown in Figures 4.34a and 4.34b. As the simulation shows, the error increases to 2.5 % close to the power supply rails. However, considering the requirement of the digitization range (0.8 V), the linearity of the amplifier within this range is adequate.

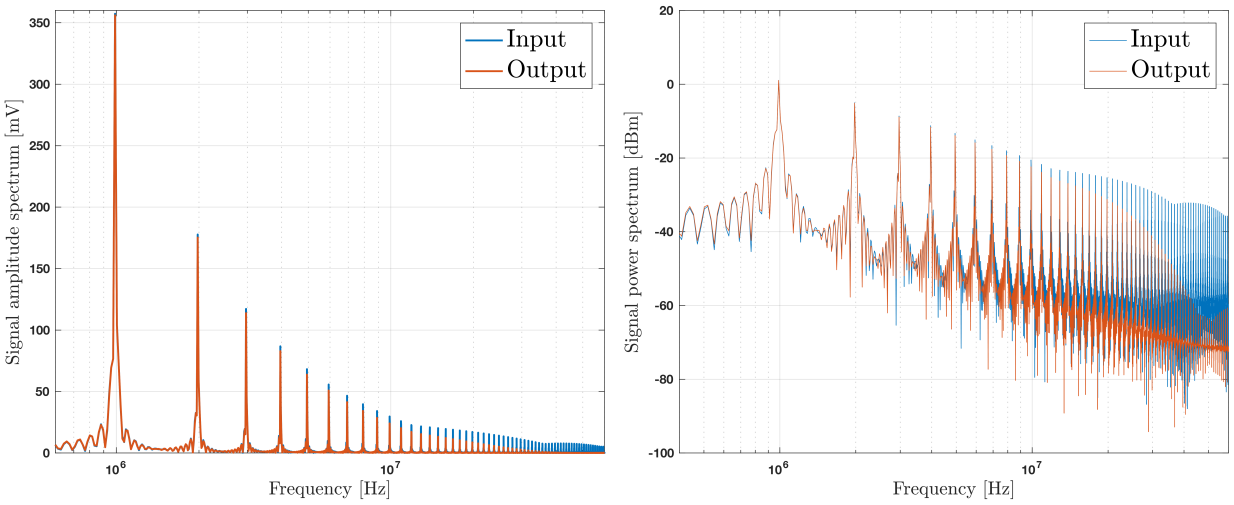


(a) (b)

Figure 4.34: (a) Transient simulation of the buffer with ramp generator. (b) Relative error of the buffer as a function of time varying input voltage.

By performing a Fourier analysis on the amplifier input and output transient response, the signal power spectrum was obtained as shown in Figure 4.35. From this data, the large signal

bandwidth of the amplifier has been found to be 13.9 MHz, as shown in Figure 4.36. By observing the ramp signal in 4.34a we can conclude that the large signal bandwidth is dominated by distortion due to compression at the output.



(a) (b)

Figure 4.35: (a) Signal amplitude spectrum of the ramp buffer as a function of frequency. (b) Signal power spectrum of the ramp buffer as a function of frequency.

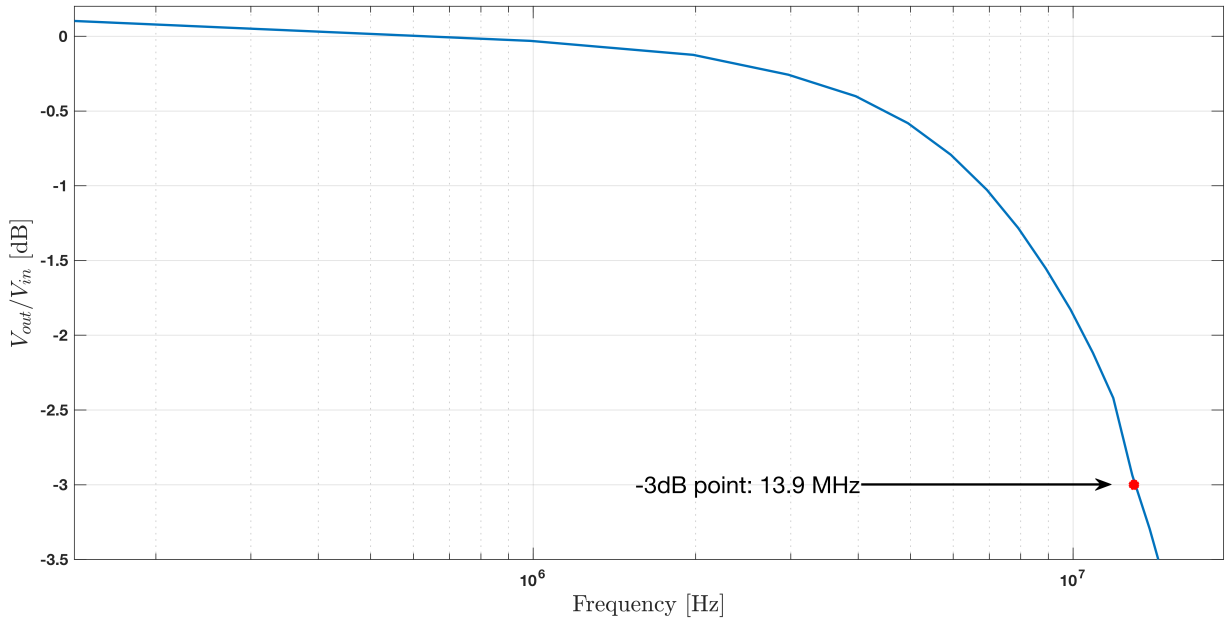
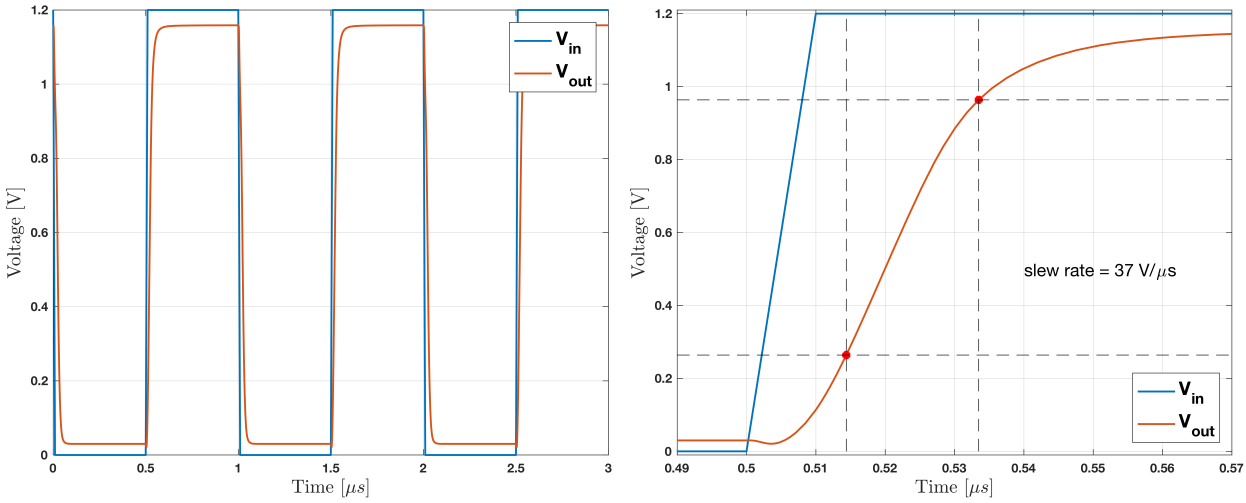


Figure 4.36: Large signal bandwidth of the ramp generator buffer.

Finally, the slew rate of the OTA was simulated by feeding a square wave into the system; the result can be seen in Figures 4.37 and 4.37b. The slew rate was found to be 37 V/µs, which makes the amplifier fast enough to drive the 1 µs ramp.



(a) (b)

Figure 4.37: (a) Transient simulation with square wave input. (b) Slew rate of the buffer amplifier.

A summary of the buffer amplifier performance parameters is given in Table 4.5. The OTA layout was drawn as shown in Figure 4.38.

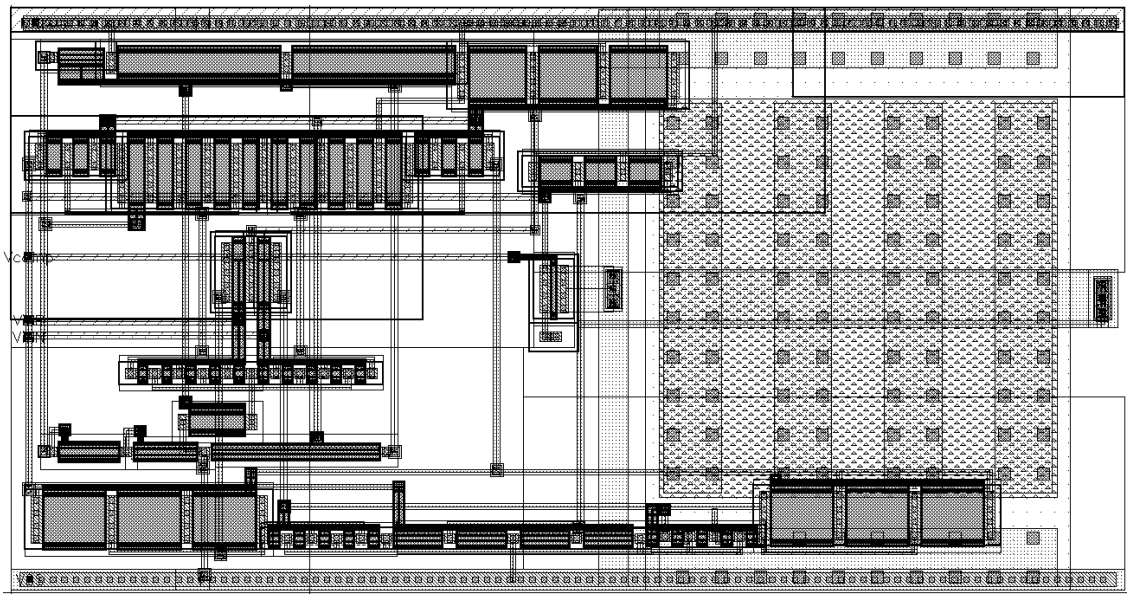


Figure 4.38: Layout of the buffer for ramp generator.

Table 4.5: Summary of the ramp generator buffer performance.

Specification	Target	Result
Small signal bandwidth	167 MHz	
Phase margin	67°	
Large signal bandwidth	13.9 MHz	
Max linearity error 0.1 V ⇒ 1.1 V	1.4 %	
Slew rate	37 $\frac{V}{\mu s}$	

4.2 Simulation results

After developing and individually evaluating each of the sampling unit components, all of the parts have been combined to form the actual sampling unit. The full sampling unit schematic shown in Figure 4.39.

First, the steps taken in testing the operation range are listed below:

1. A 1 µs ramp voltage from 0 V to 1.1 V, generated by the ramp generator and buffered by the buffer, is applied into the non-inverting inputs of 64 comparators. Each comparator output is connected to a capacitor, which emulates a 27.1 fF load (equivalent to the FIFO register input capacitance).

2. A constant DC voltage is applied into the inverting input of each comparator; this voltage is swept from 0 to 1.2 V.

3. The operating range is achieved by observing the triggering of the comparator. For this design, the operating range is from 50 mV to 1.1 V.

4. The results of this test are shown in Figure 4.40.

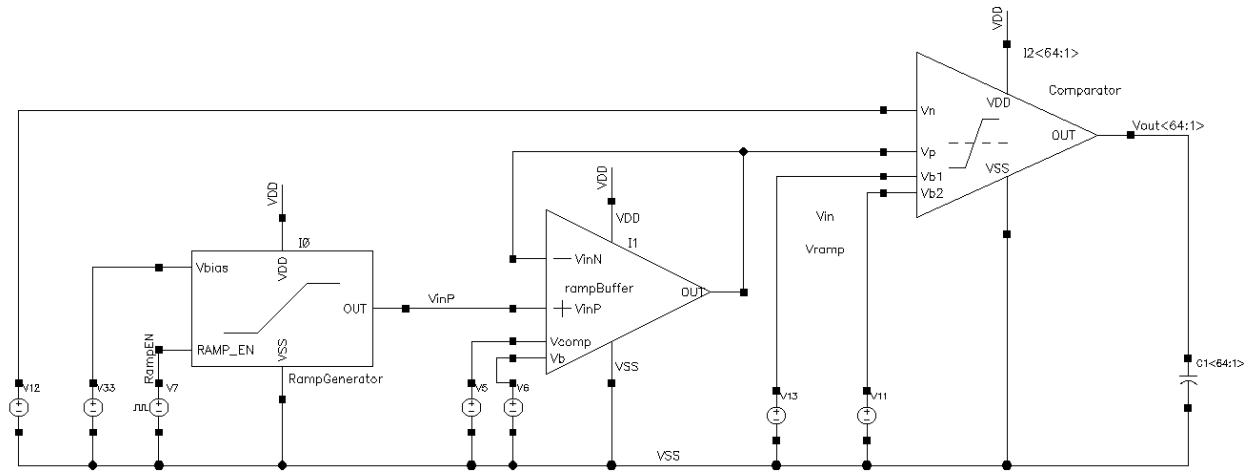


Figure 4.39: Test bench for testing the full sampling chain.

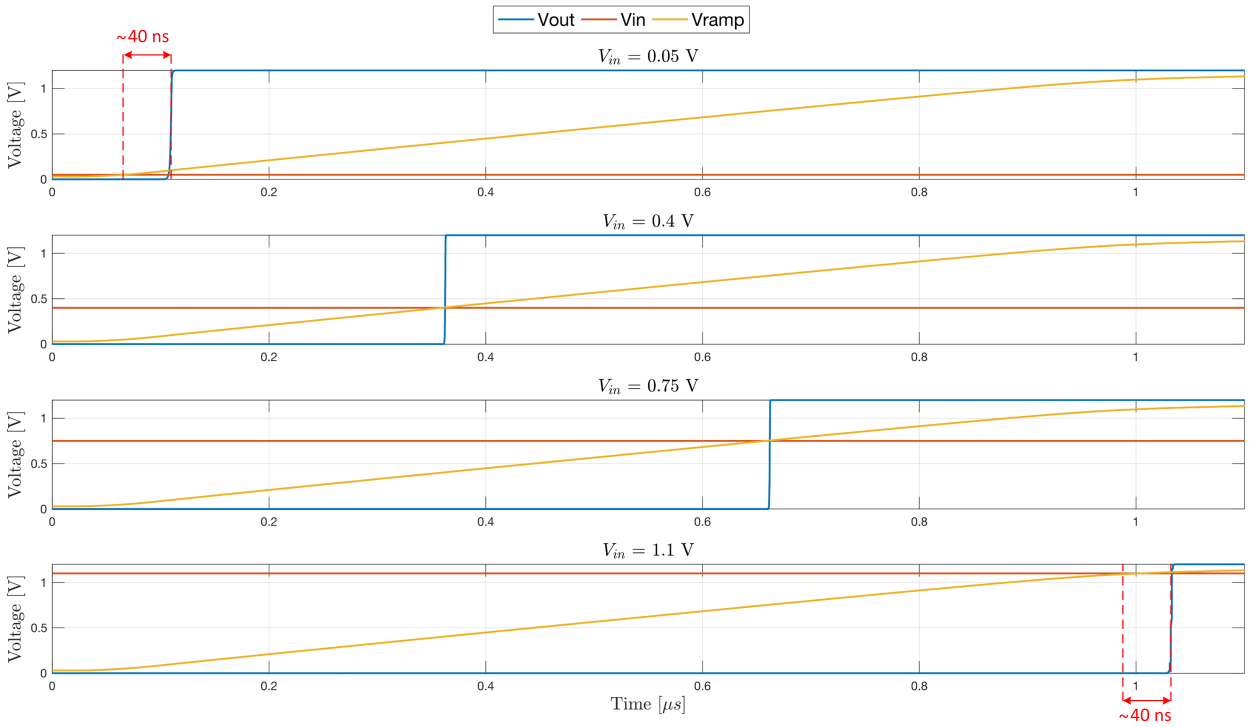


Figure 4.40: Transient simulation for evaluating the full sampling structure

Second, the linearity test was performed. The steps for the linearity test are:

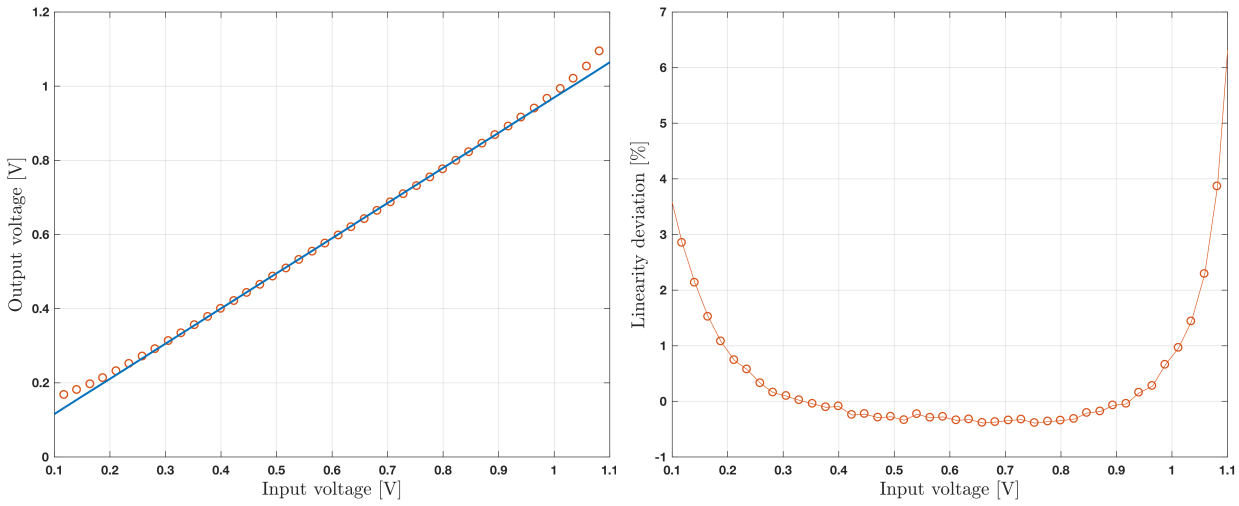
1. The DC input voltage of the comparator is swept from 0 V to 1.2 V.

2. The ramp generator is enabled.

3. When the ramp generator triggers the comparator, the time of the triggering event is saved.

4. The result is obtained by multiplying the ramp slope by the triggering time.

5. The linearity test results are shown in Figure 4.41.



(a) (b)

Figure 4.41: GRAPH ASIC Wilkinson ADC output voltage as a function of the input voltage. (b) Relative error of the Wilkinson ADC as a function of the input voltage.

As the Figure 4.41b shows, the linearity of the sampling unit response over the dynamic range (0.2 V to 1 V) is very linear. The degradation of the linearity at the edges of the dynamic range is solely due to the comparator and not the ADC itself. As mentioned before, most of the error originates from the non-constant propagation delay of the comparator, which can also be observed in Figure 4.40, where the propagation delay is approximately 40 ns while operation close to the power supply rails. If better linearity is desired further improvement of the comparator is necessary, however, this would lead to a higher power consumption, which is not desirable. Alternatively, this error can be calibrated.

Figure 4.42 shows a comparison between the GRAPH and HG2 responses in terms of linearity over the 0.8 V dynamic range. As the result shows, the absolute maximum observed deviation in the GRAPH linearity curve is only 0.7 %, whereas for HG2 it is 1.8 %. This results in an improvement of the linearity by approximately 61 %.

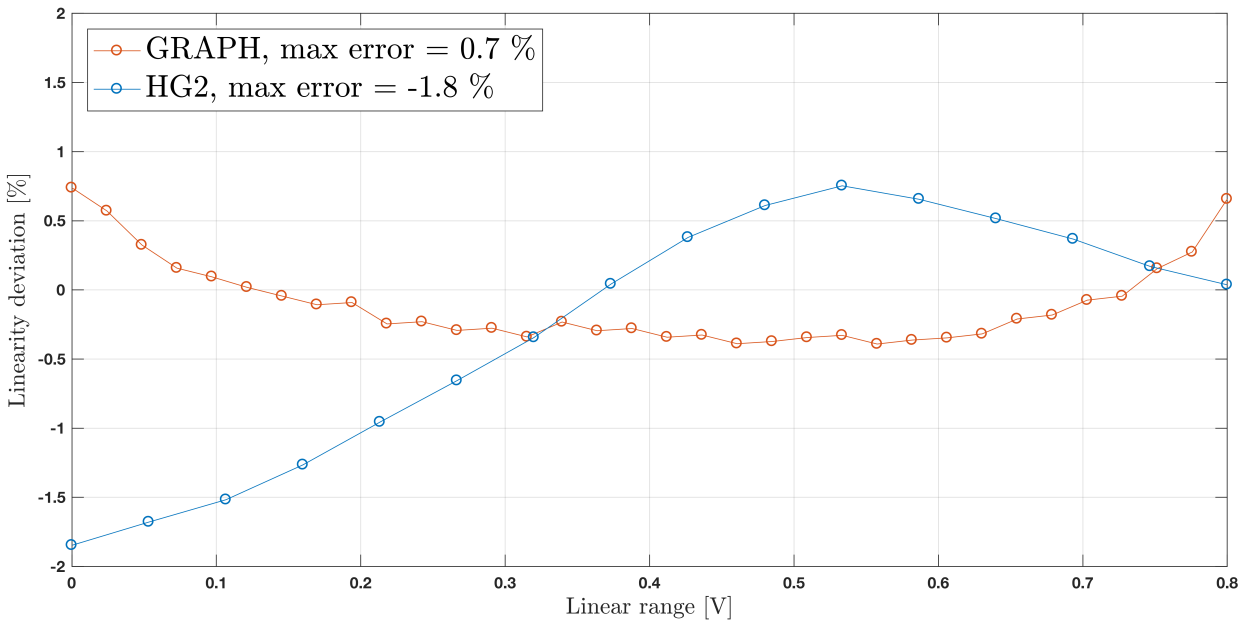


Figure 4.42: Linearity comparison of HG2 and GRAPH over 0.8 V range

4.3 Power consumption

The power consumption was simulated by using the test setup presented in Figure 4.39. While all of the active components have been included in the simulation, the sampling cell was not part of them. Due to its circuit structure, the sampling cell is passive and does not draw any significant amount of current, other than leakage. The total current draw for one sampling window as a function of input sampled voltage is shown in Figure 4.43. For the operation range of 0.8 V, the average current draw is 320 µA. This leads into a mean power consumption of 5.12 mW for 16 channels.

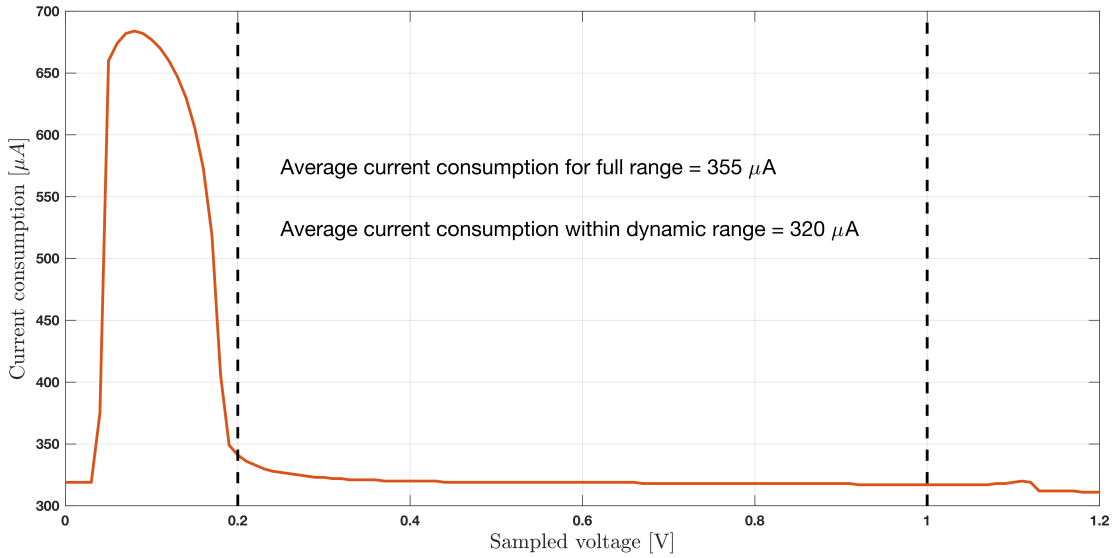


Figure 4.43: Total current draw of one sampling window as a function of input sampled voltage for GRAPH ASIC. The operation range is 0.8 V.

It should be noted that sampling the signals with voltages below 0.2 V increases the current draw significantly. As seen in Figure 4.44, this is caused by the operation of the comparator. However, since the operation range for this ASIC is from 0.2 V to 1 V this effect can be minimized by applying a bias voltage of 0.2 V or greater into the input signal.

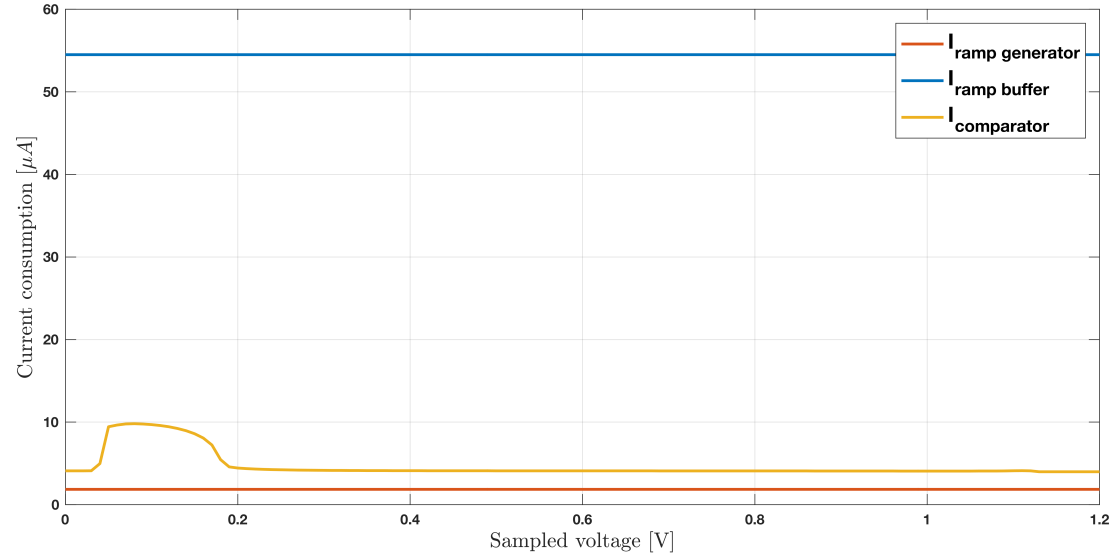


Figure 4.44: Current draw of individual components in sampling window as a function of input sampled voltage for GRAPH ASIC. The increased current draw in low sampling voltage is caused by the comparator.

CHAPTER 5
FUTURE WORK

The sampling structure, as presented in this thesis, is already a major part of the chip design. However, there are still some key components as well as design challenges to overcome before the GRAPH ASIC can be submitted for manufacturing. Firstly, the CSA output buffers needs to be re-optimized to be compliant with the new integrated CSA/digitizer ASIC. This component will bring significant power savings compared to the previous designs, since GRAPH ASIC does not need to drive the signal outside the chip and into the digitizer anymore. This means the capacitive load that is needed to be driven by the buffer is significantly lower.

Secondly, the timing generator needs to be re-designed to be compliant with 130 nm process. This component can be designed in the same fashion that is presented in Section 3.1.3, however, new more efficient methods are under research.

Thirdly, the digital storage and its controlling logic needs to be implemented. This design is an ongoing design process and it consists of a memory write access logic, which controls where in the storage the data will be stored; the memory itself, consisting of 32 registers leading to 24576 bits of memory; memory read access logic, which controls where in the memory the data is be shifted out; FIFO registers that buffer the data outside the chip.

Finally, the floor plan of the ASIC needs to be finished, where all designed components are combined into one integrated circuit. The integration of the CSA and the waveform digitizer is one of the major milestones of this project. The work for the floor plan have already been started and a 128-pin QFN is the choice of package.

CHAPTER 6
SUMMARY

This thesis discusses the construction and testing of cross strip micro channel plate detector readout system electronics with the intention of increasing NASAs technology readiness level, thus enabling prototyping for the future space missions. In the first phase a 16-channel trans-impedance amplifier ASIC (CSAv3) was designed and developed. This component converts the collected charge from the detector into measurable voltage pulses, which are subsequently digitized by a waveform sampling ASIC (HalfGraph2). The post-processing of the information is done on FPGAs and the results are transferred to a computer for analysis. After the success of the first phase, the scope of the second phase is to further integrate the readout system by combining these two ASICs into one high-density, low-power, front-end mixed-signal amplifier/digitizing ASIC, while further improving the design of the individual parts to decrease the material budget, lower the power consumption, improve the performance, and ultimately reduce the physical footprint.

This thesis includes partial characterization of the phase one electronics and the development of some of the key components for the GRAPH ASIC, which is planned to be manufactured in the near future. The phase one characterization results show that the phase two electronics can further improve the device performance by improving the linearity of the individual components. In addition, by scaling the device into smaller technology the power consumption can be reduced significantly.

The development of the second phase integrated electronics involve the re-design of the waveform digitizing ASIC from a 250 nm process to be compliant with 130 nm process. This technology node change raised some design challenges, which were the main focus of this thesis. More specifically, as the CMOS devices are scaled to smaller sizes, the power supply rails, channel lengths, and gate oxide thicknesses decrease, leading to larger transistor leakage currents. Thus, the device scaling limits the dynamic headroom, due to limited power supply rails, of the circuitry and increase both static power consumption and non-linearities in the analog memory storing due to the leakage current.

In order to meet the new design requirements, new design approaches for the sampling structure were taken. This new design is still based on switched capacitor arrays as its predecessor HalfGraph2, however, the transferring of sampled data to a storage array has been replaced with direct digitization of the samples. The digitized data is then stored in a digital memory buffer, which does not suffer from the leakage issues. The technology change lead into new strict design requirements for each individual component design. These requirements were met with each individual component, leading into the total digitization linearity increase of 61 %.

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